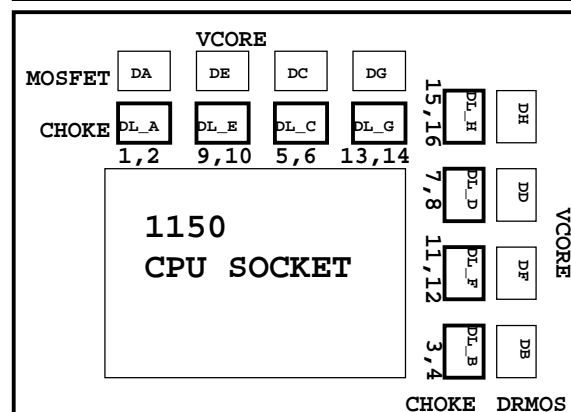
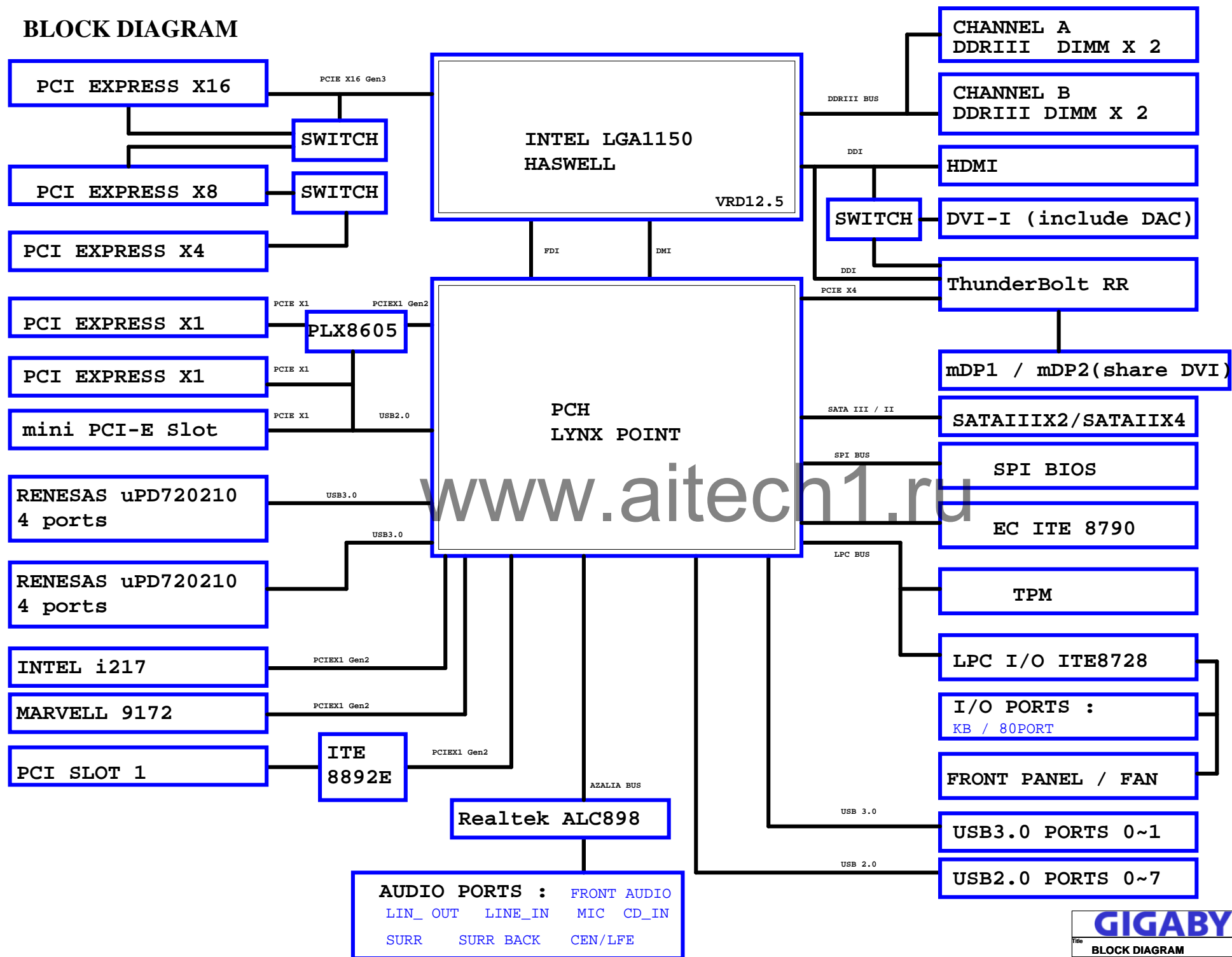


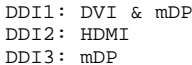
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04-06	CPU_LGA1150
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	HDMI / DVI (Switch) / TPM
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*8 SLOT
17	PCI EXPRESS SWITCH X16/X8/X4
18	PCI EXPRESS*1 SLOTS X2
19	PCI EXPRESS*4 SLOT
20	ITE 8892
21	PCI SLOT 1
22	Dual BIOS
23	ALC898
24	REAR AUDIO JACK
25	AMPLIFIER
26	IR3563B PWM
27-28	IR3550 VCORE 16 Phase
29	IR3570 PWM
30	IR3598 DDR 2 Phase

31	5VDUAL, 3VDAUL, ERP
32	PCH1.05V, PCH1.5V, VCC3_DAC
33	I/O ITE8728
34	USB3 , KB/USB3
35	F_PANEL , F_USB , PHOT
36	F_USB 2.0
37	F_USB 3.0
38	ATX POWER, CLOCK GEN
39	HWM, FAN CTRL
40	INTEL I217 Lan
41	Marvell 9172
42	RST, PWR, CLR_CMOS
43-44	USB3.0 HUB uPD720210
45-46	USB3.0 HUB_B uPD720210
47	PLX8605
48	mini PCIE Slot
49	EC ITE 8790
50	DVI / mDP Switch 412
51-54	Thunderbolt RR 4C



BLOCK DIAGRAM





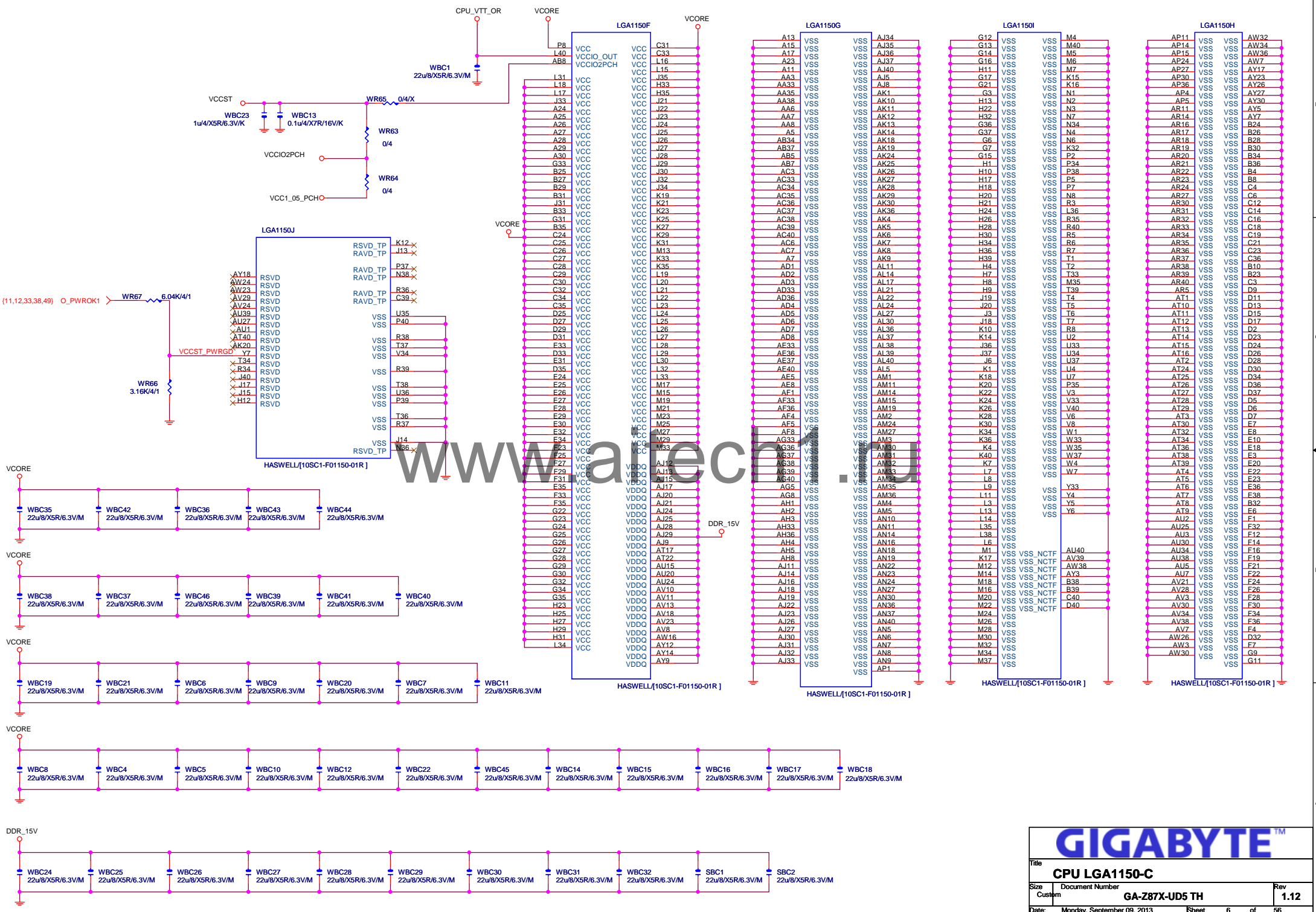
HASWELL/[10SC1-F01150-01R]

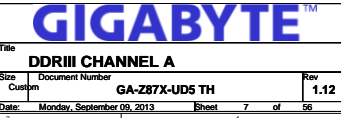
HASWELL/[10SC1-F01150-01R]

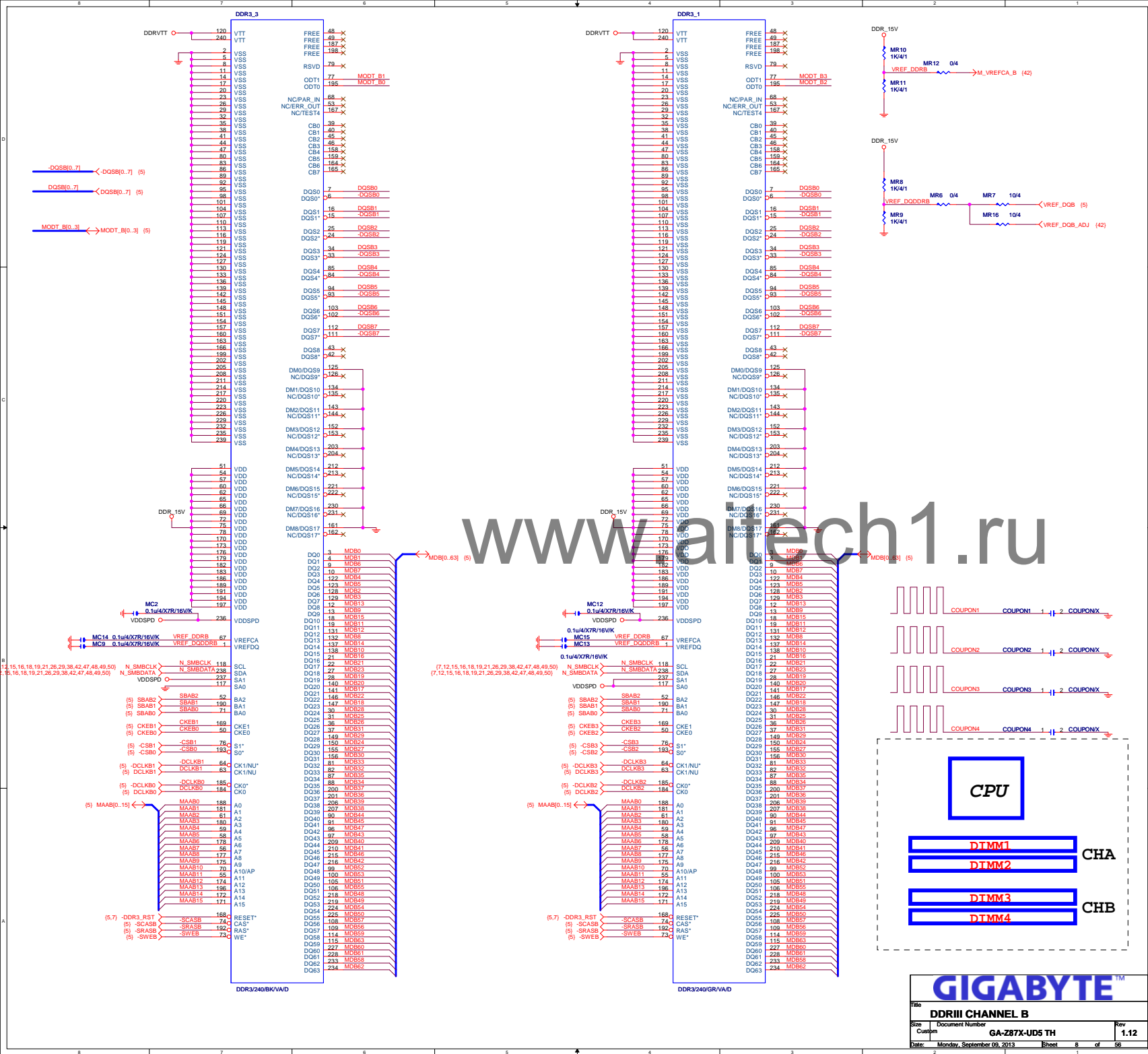
LGA1150
ILM_BP/1156/BKNV/[12KRC-0F0001-61R]

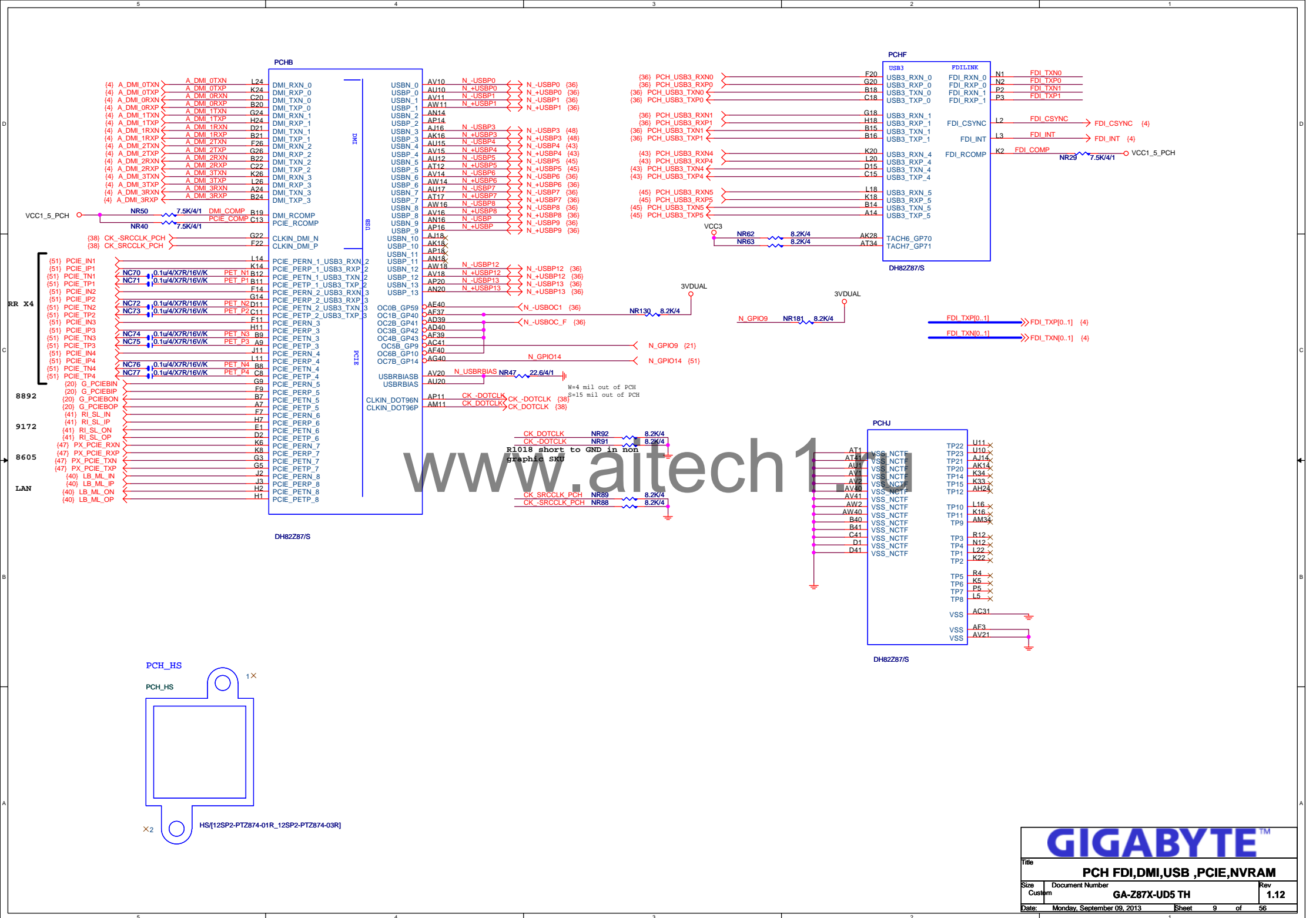
Need check the new CPU M

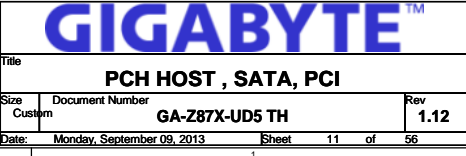
Place in CPU bottom side

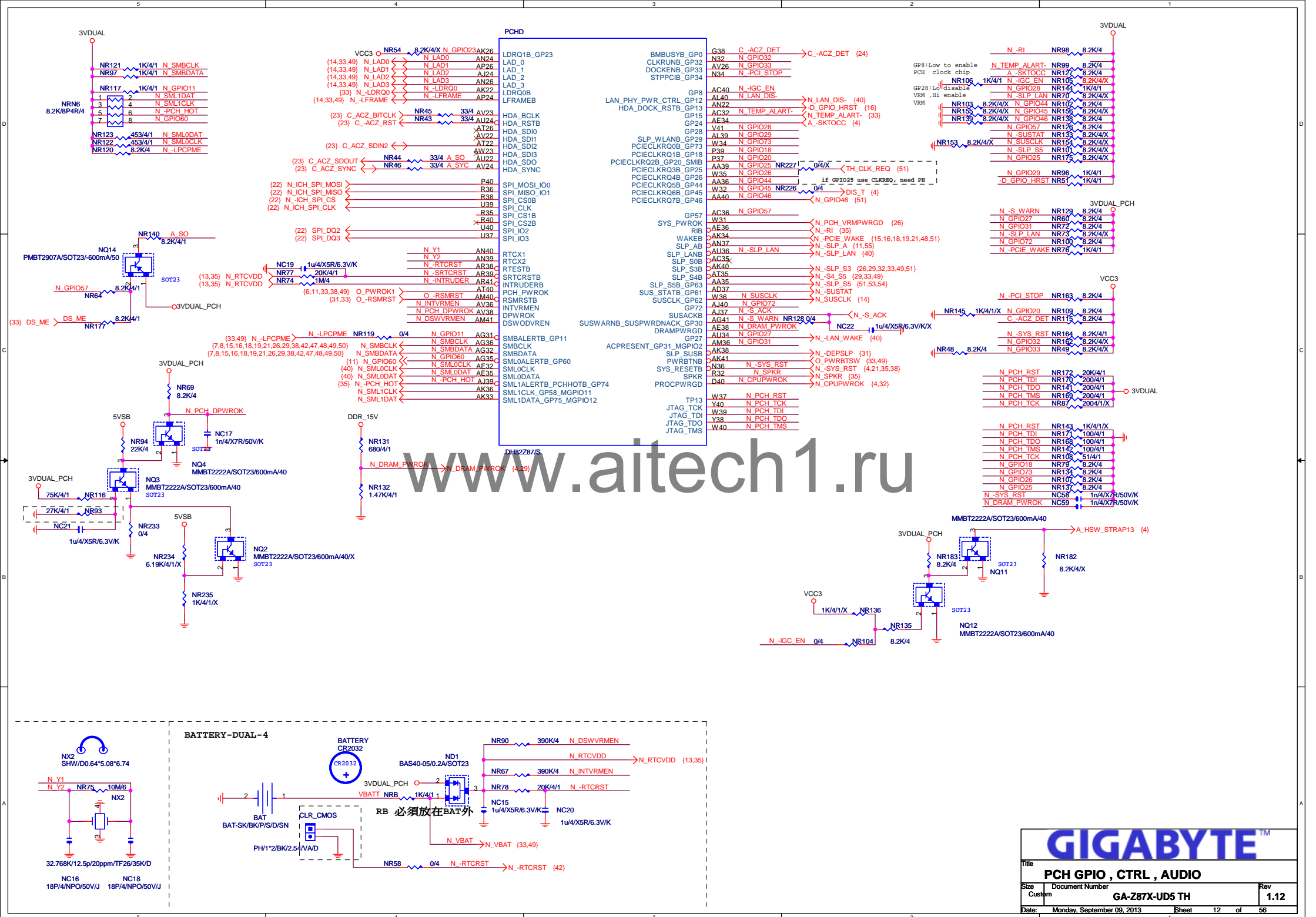




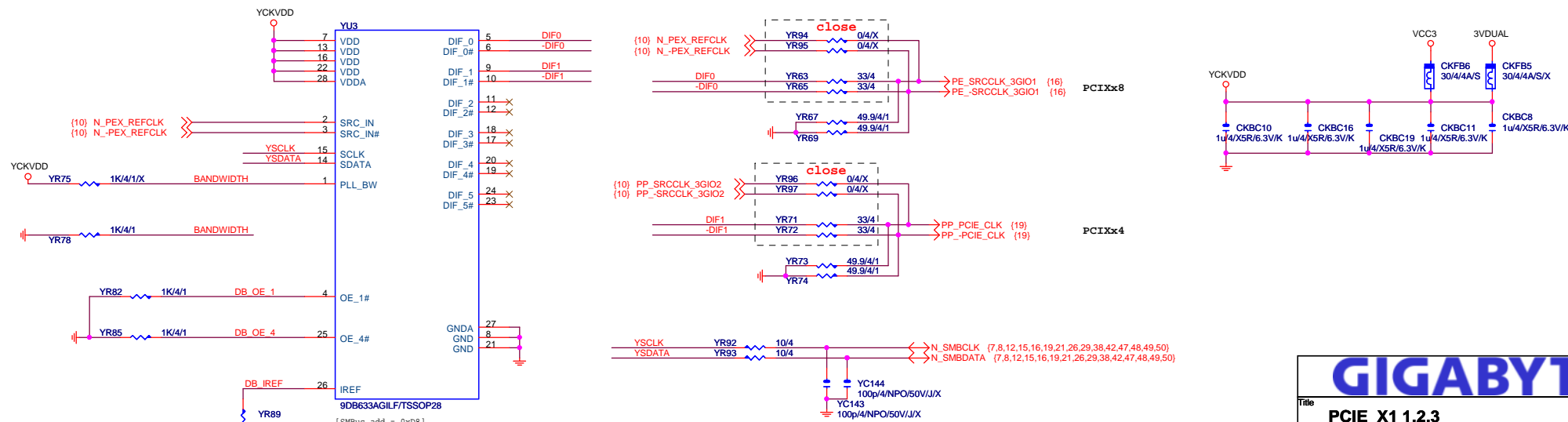
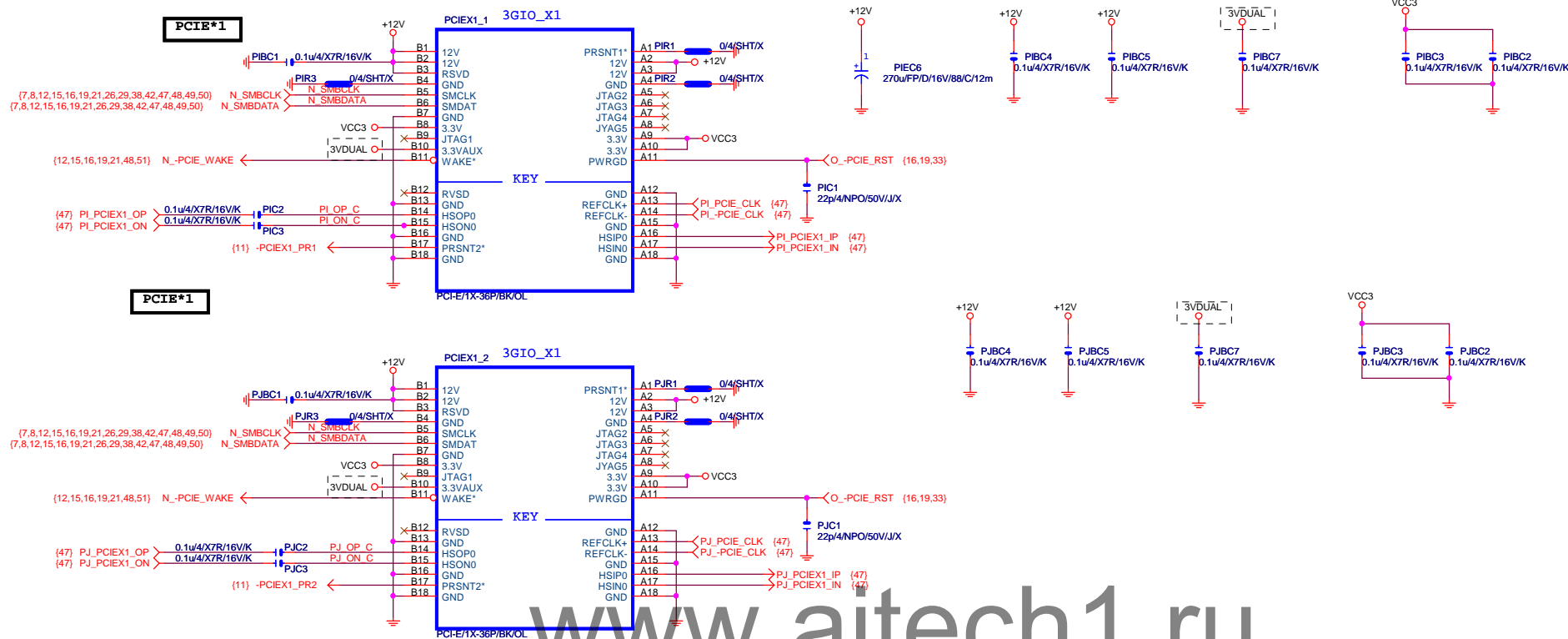




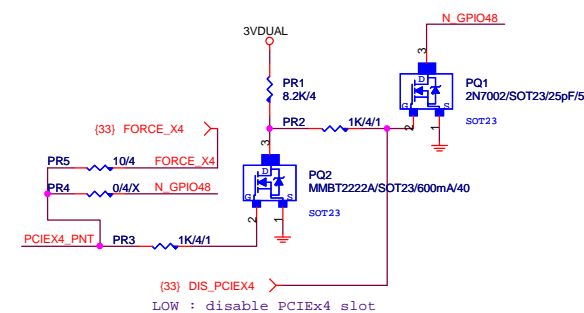
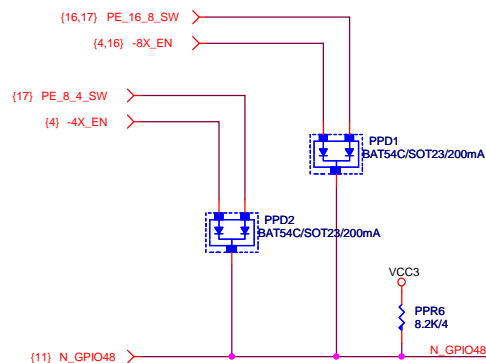
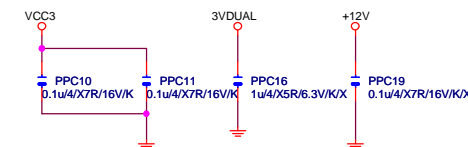




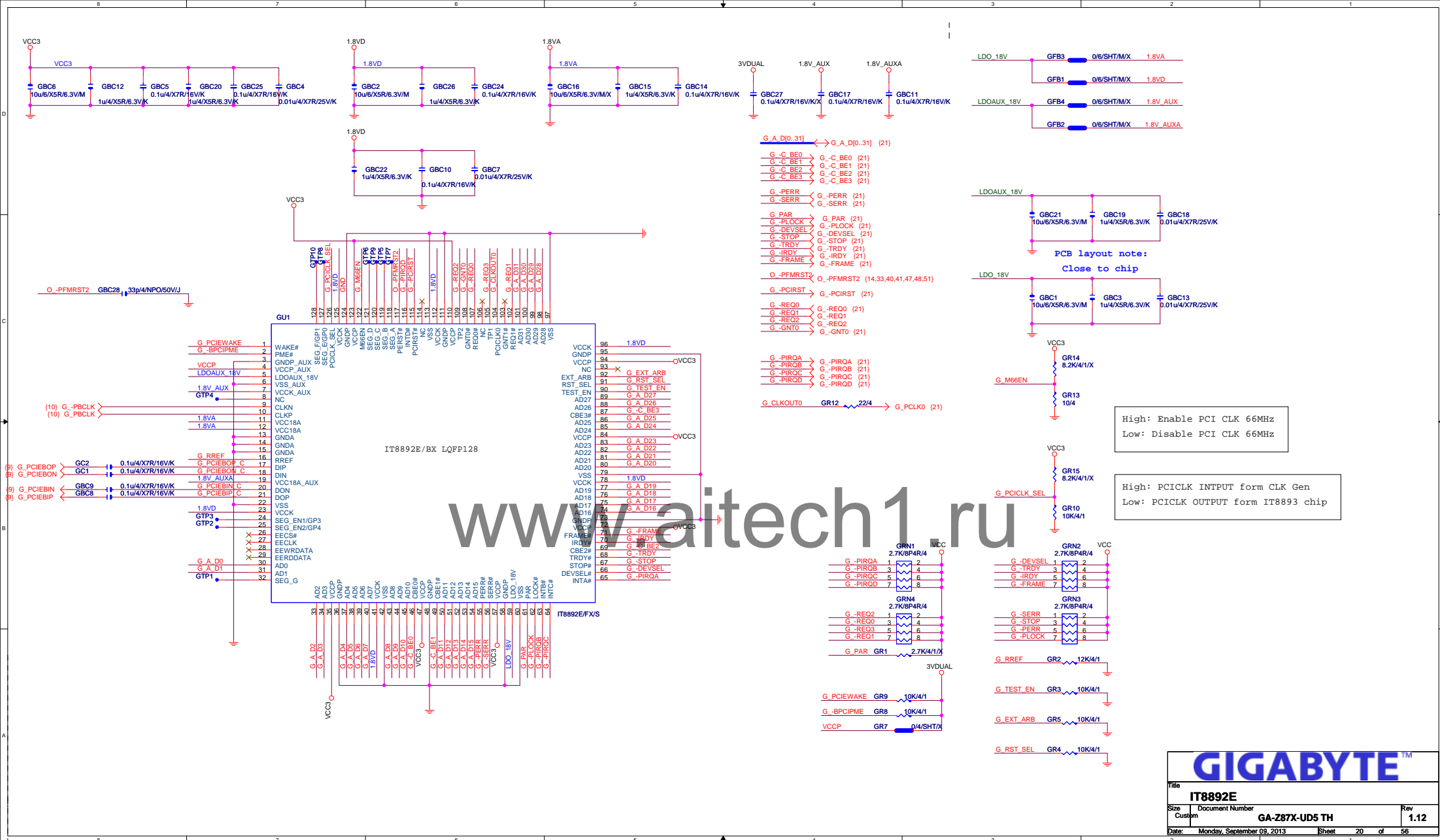




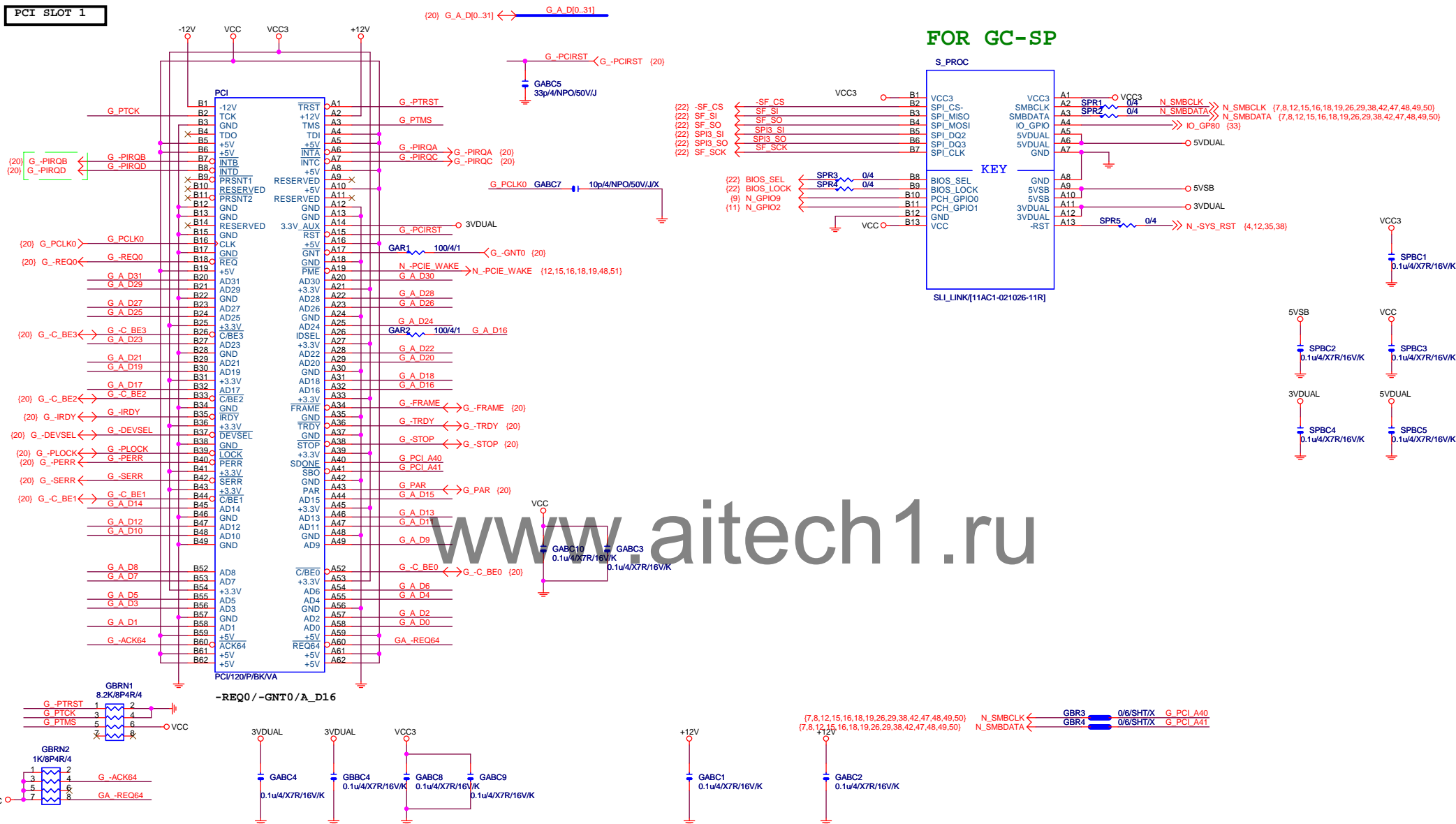
PCIE*4



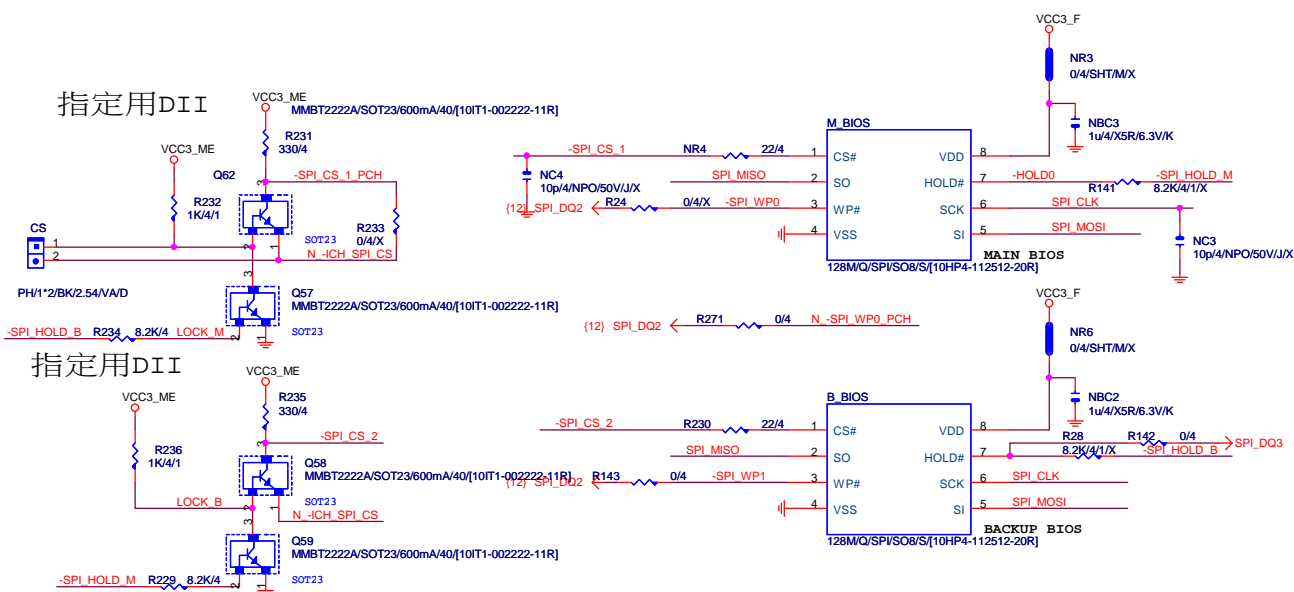
PP_EXP_SW_RXP[12..15] >> PP_EXP_SW_RXP[12..15] (17)
PP_EXP_SW_RXN[12..15] >> PP_EXP_SW_RXN[12..15] (17)
PP_EXP_SW_TXP[12..15] >> PP_EXP_SW_TXP[12..15] (17)
PP_EXP_SW_TXN[12..15] >> PP_EXP_SW_TXN[12..15] (17)



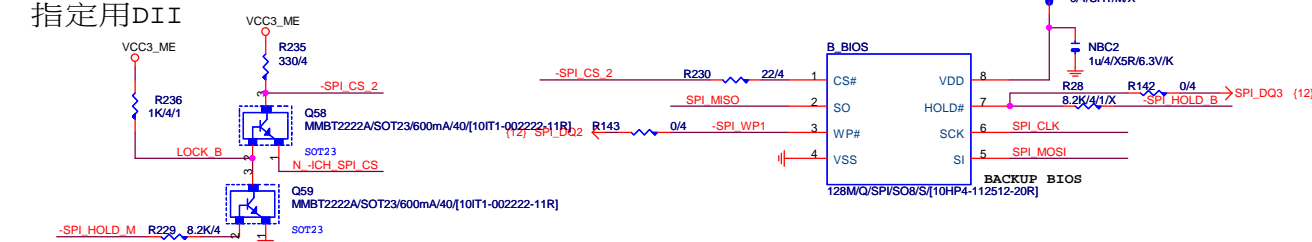
PCI SLOT 1



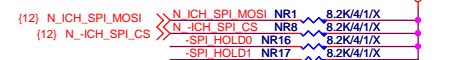
指定用DII



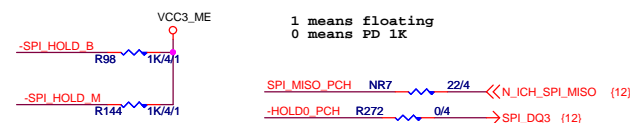
指定用DII



MOSI For DMI RX Termination Voltage

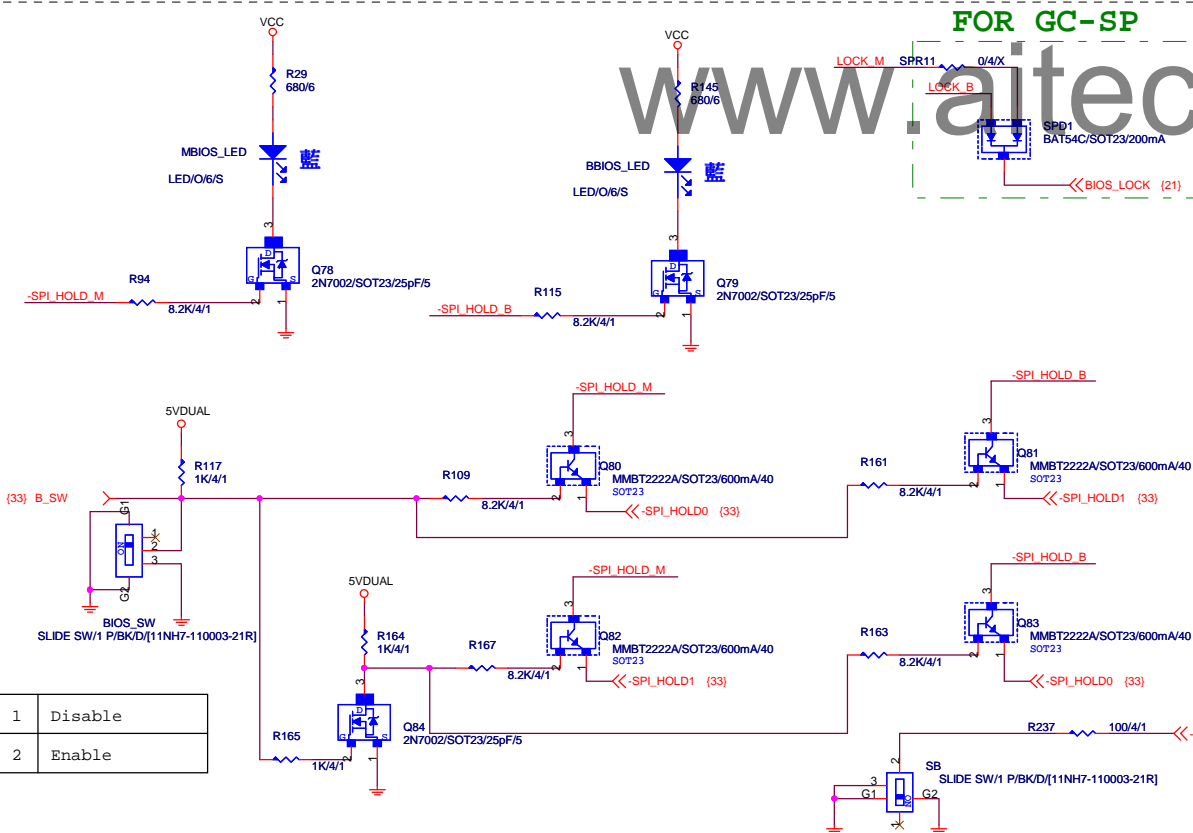


1 means floating
0 means PD 1K

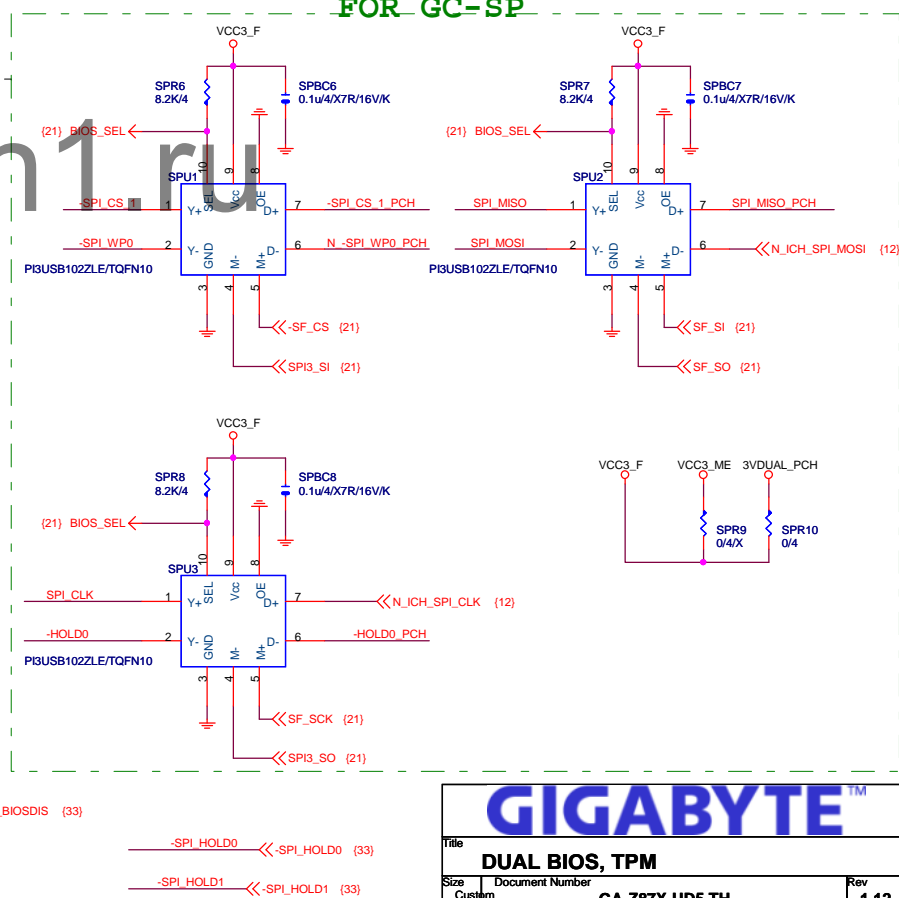


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

FOR GC-SP

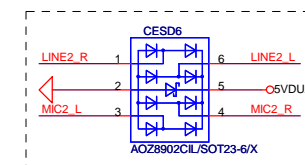
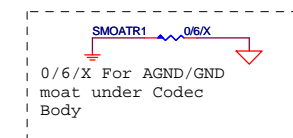
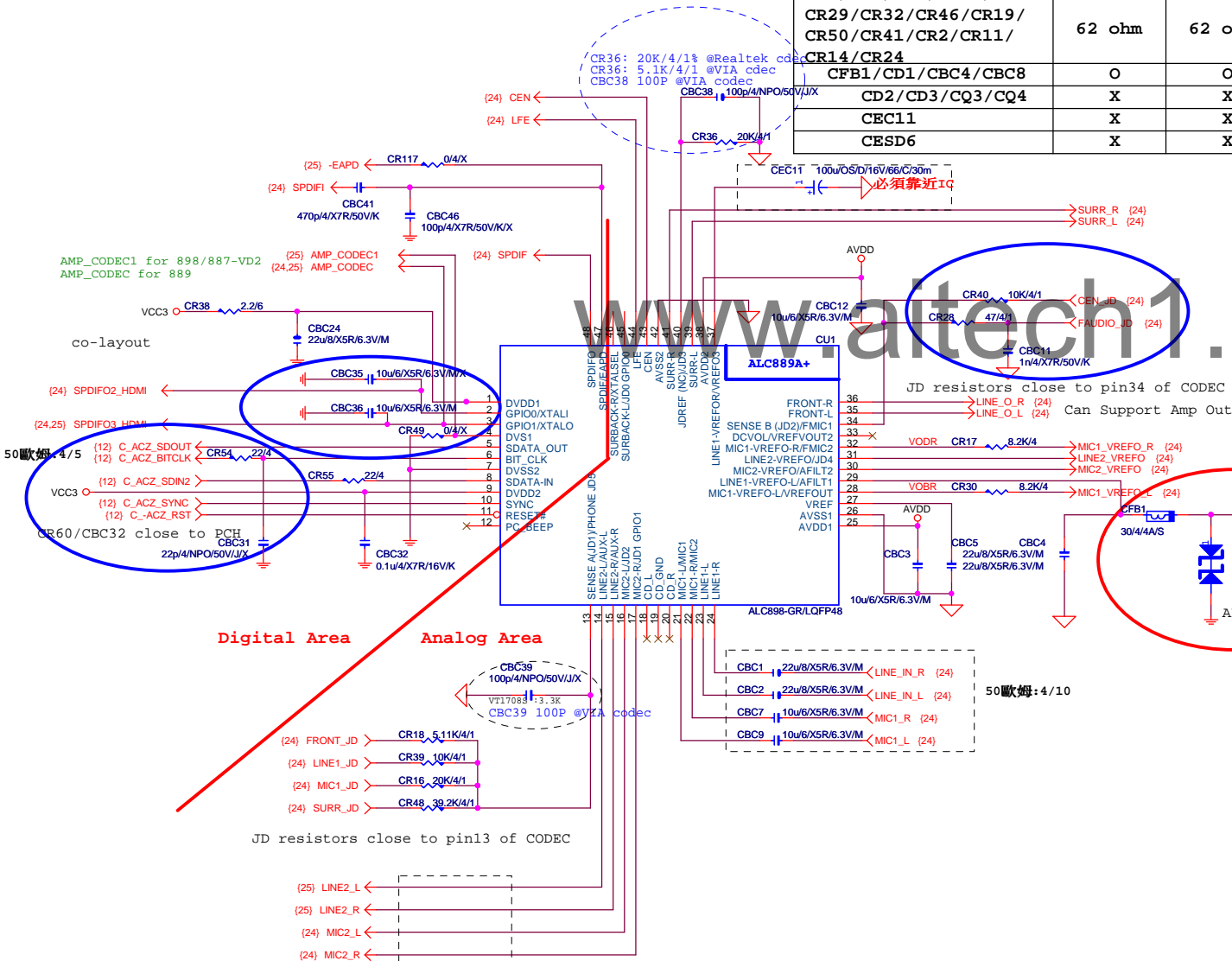


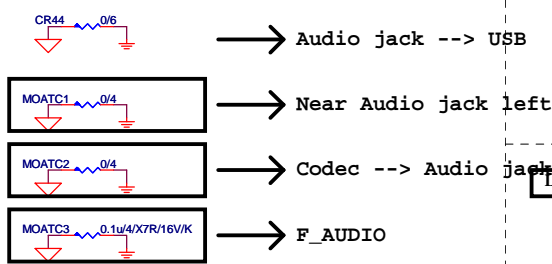
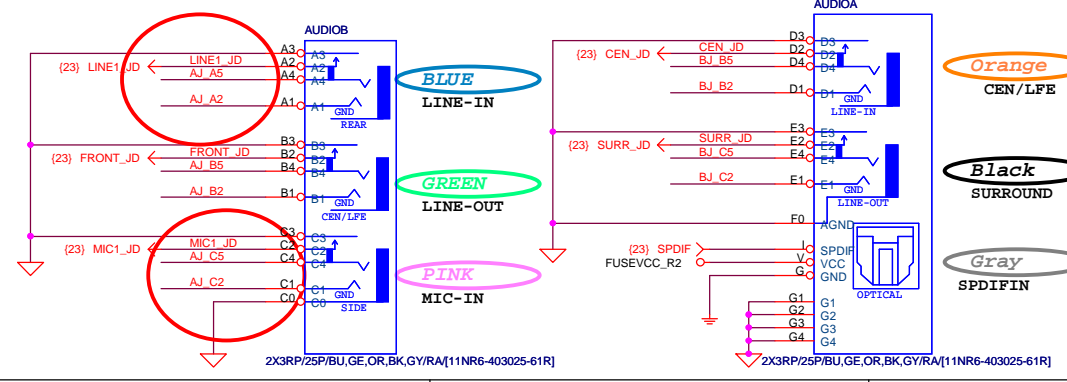
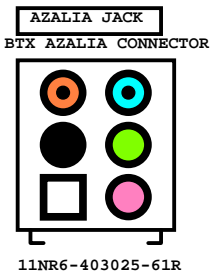
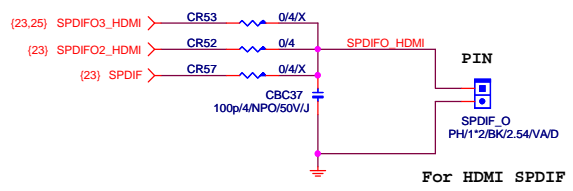
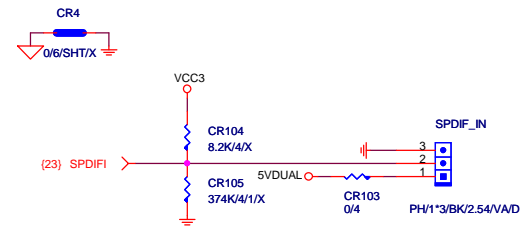
FOR GC-SP



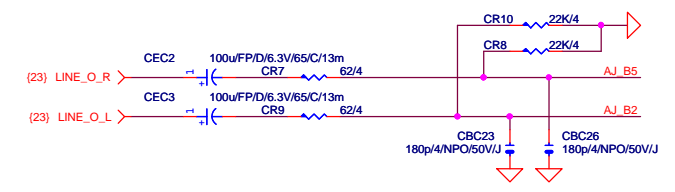
1	Disable
2	Enable

	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE	VT2021	ALC898/ALC892
CR49	X	X	O	O	X	O	X
CBC36	O	O	X	X	O	X	O
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF	47ohm+1nF
CR52	X	O	O	O	O	O	O
CR57	O	X	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R	22uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1	8.2K/4
CBC38/CBC39	X	X	X	100P/4	100P/4	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1	22K/4
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm	62 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X	O
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O	X
CEC11	X	X	X	X	X	X	O
CESD6	X	X	X	O	O	O	X

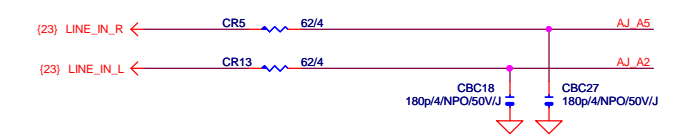




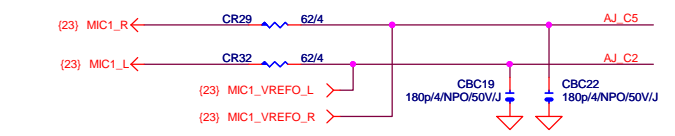
LINE-OUT



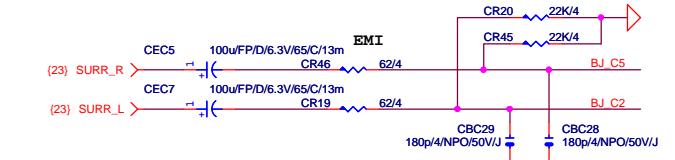
LINE-IN



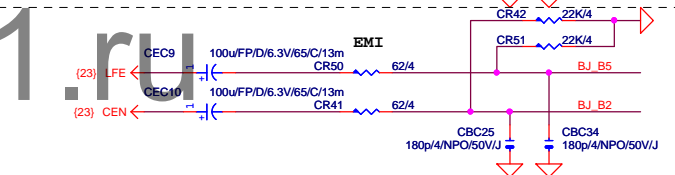
MIC-IN



SURROUND

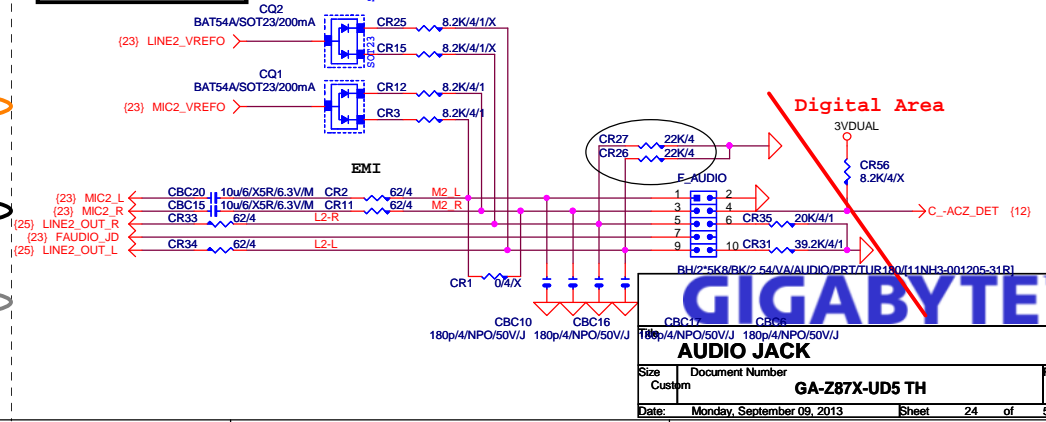


CEN/LFE



SURR BACK

AZALIA FRONT PANEL

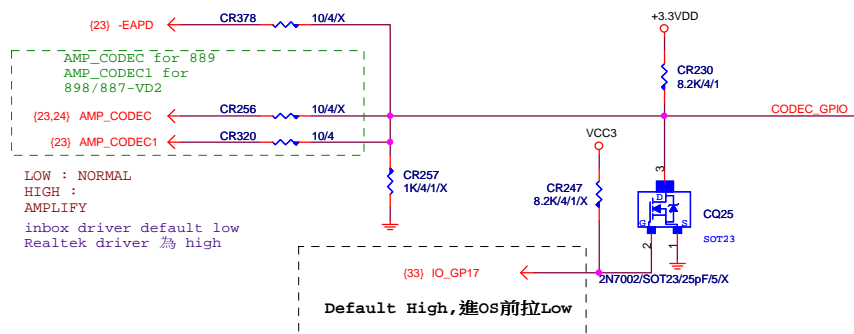
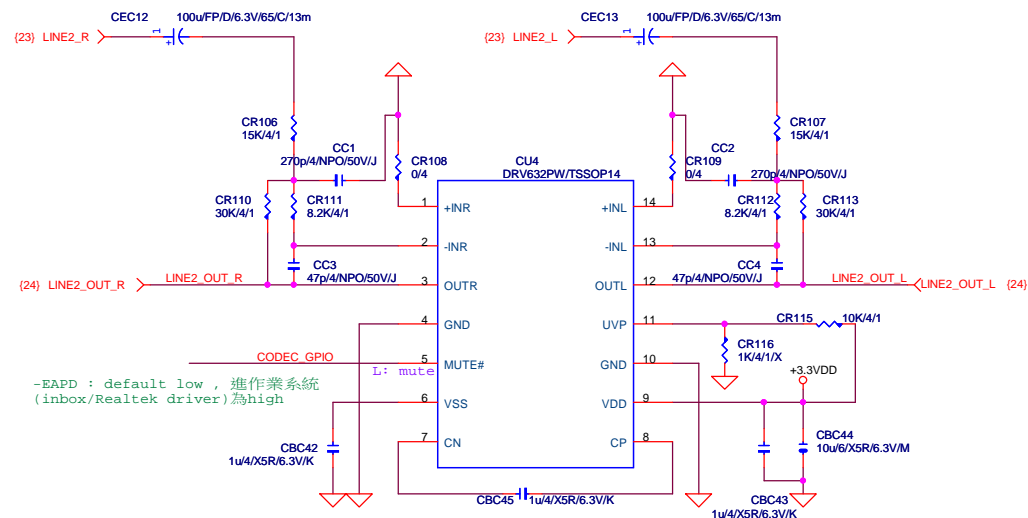


GIGABYTE

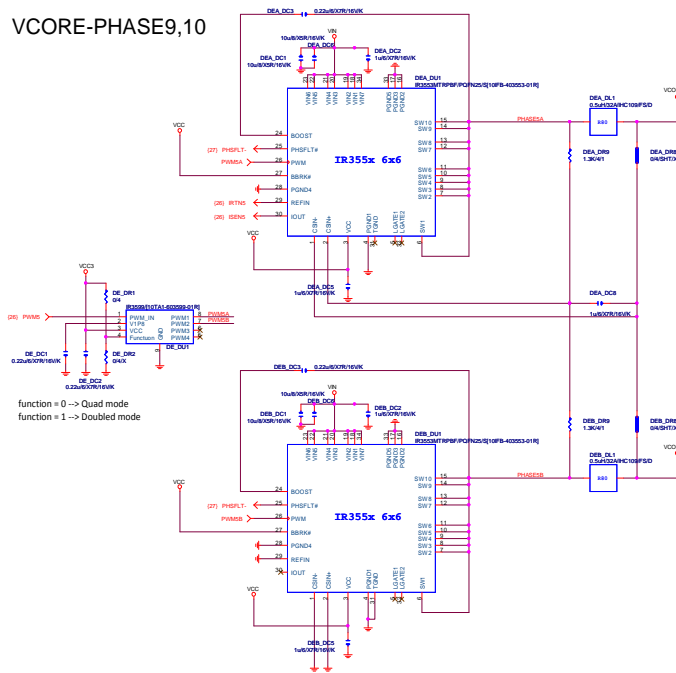
AUDIO JACK

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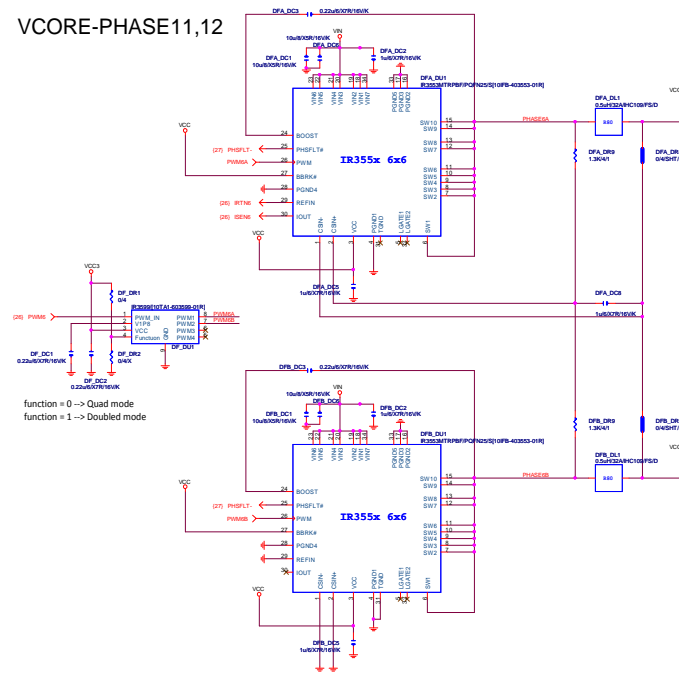
HEADPHONE



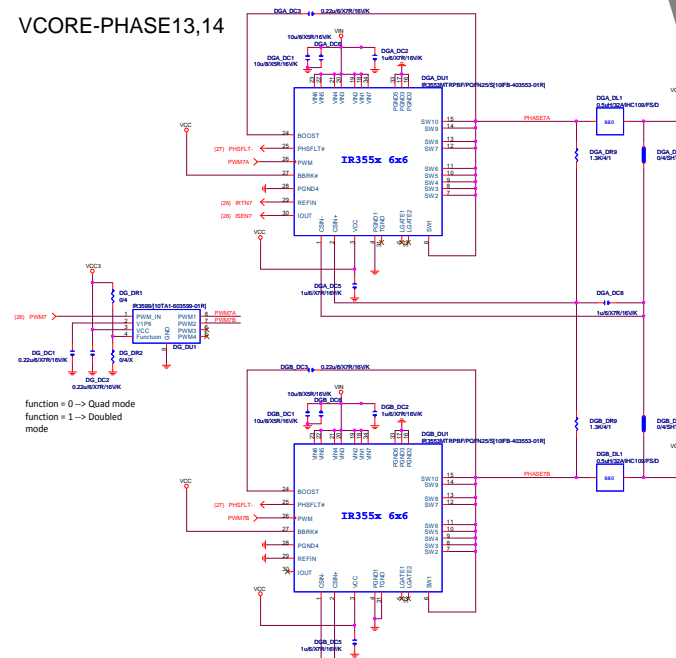
VCORE-PHASE9,10



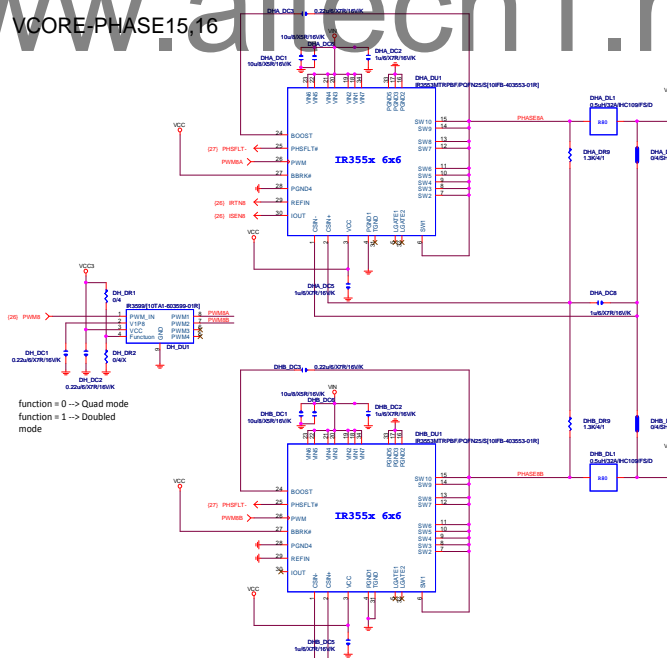
VCORE-PHASE11,12



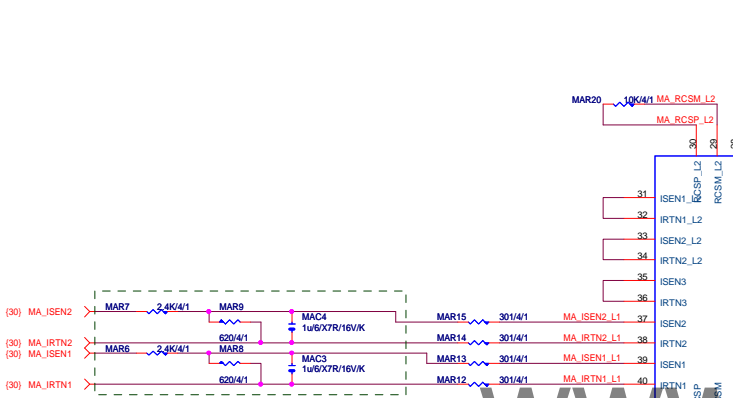
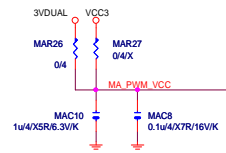
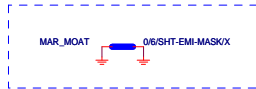
VCORE-PHASE13,14



VCORE-PHASE15,16



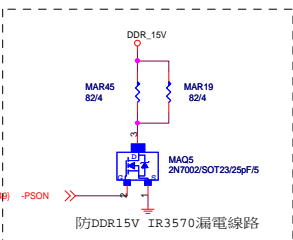
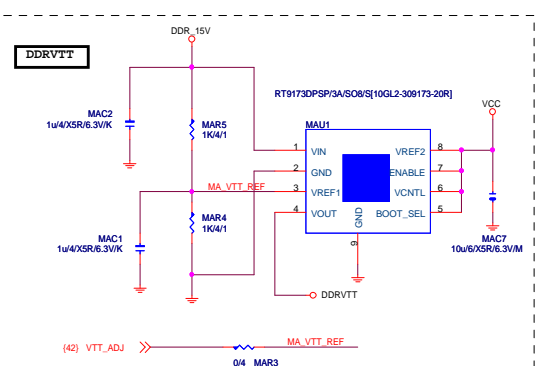
www.aitech1.ru



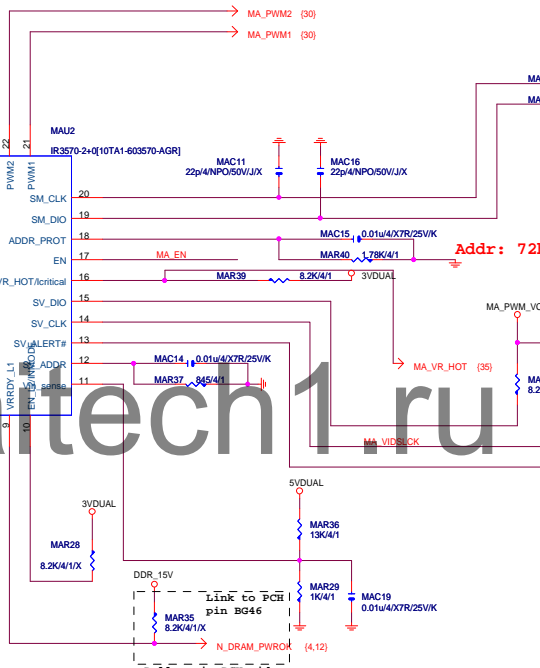
Close to DDR output inductor

should be routed as differential pair, 7mil width, 8mil spacing

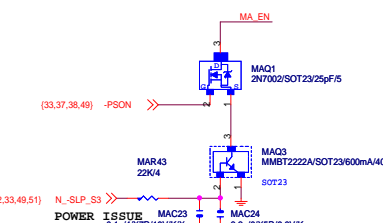
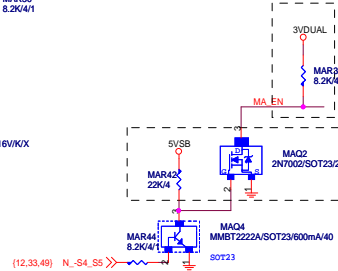
Value need check with Vendor



IR3570

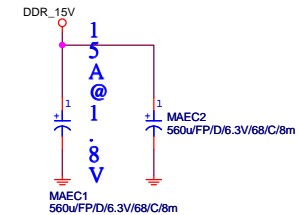
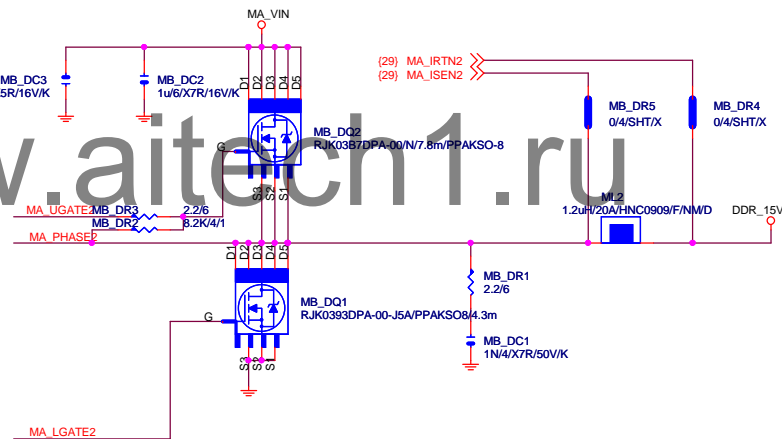
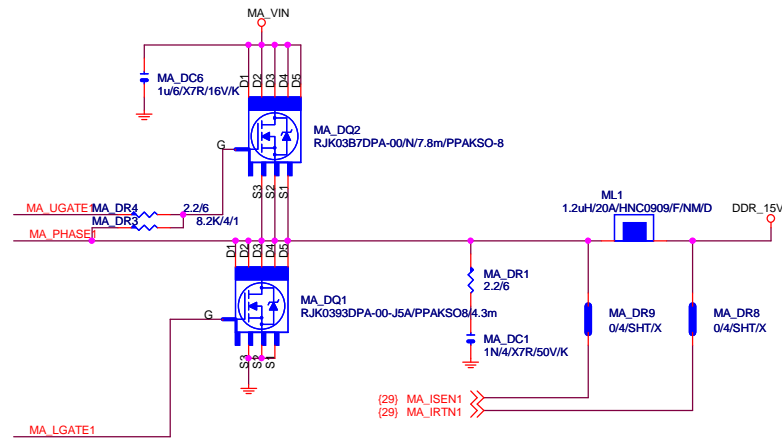
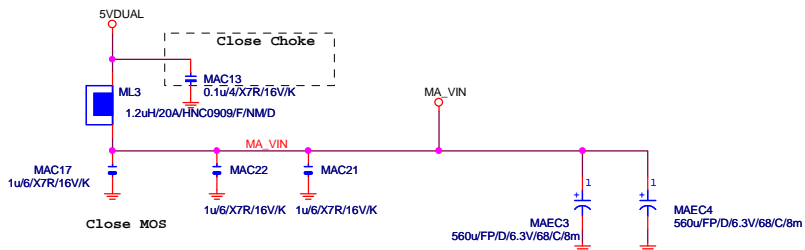
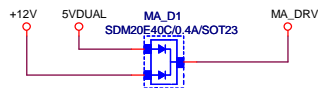
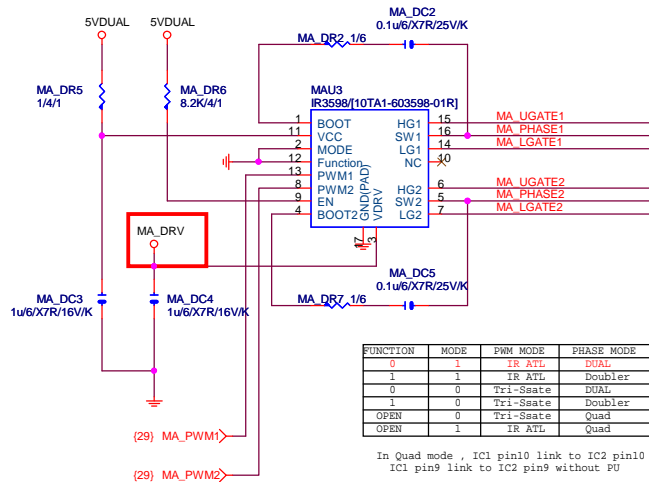


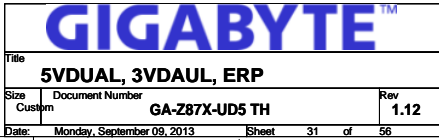
Addr: 72h



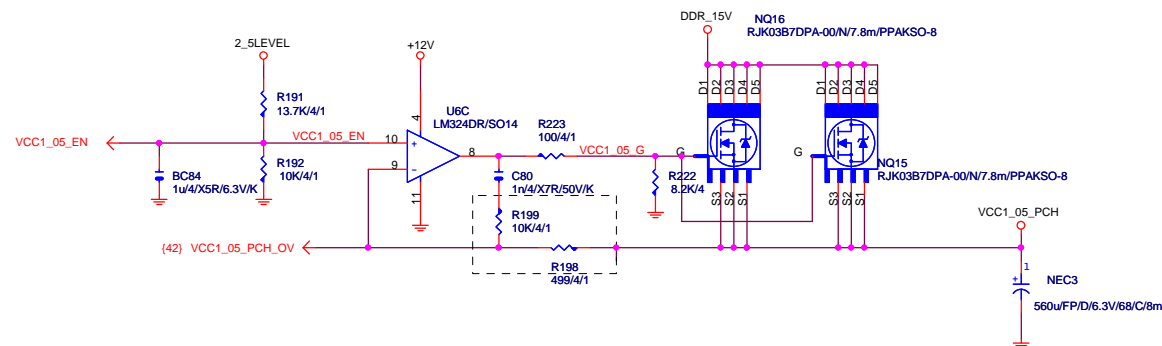
GIGABYTE™			
Title DDR POWER IR3570			
Size C	Document Number GA-Z87X-UD5 TH	Rev 1.12	
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DDR_15V

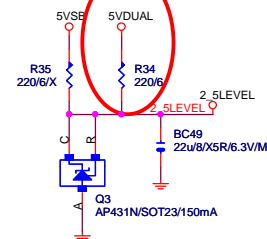




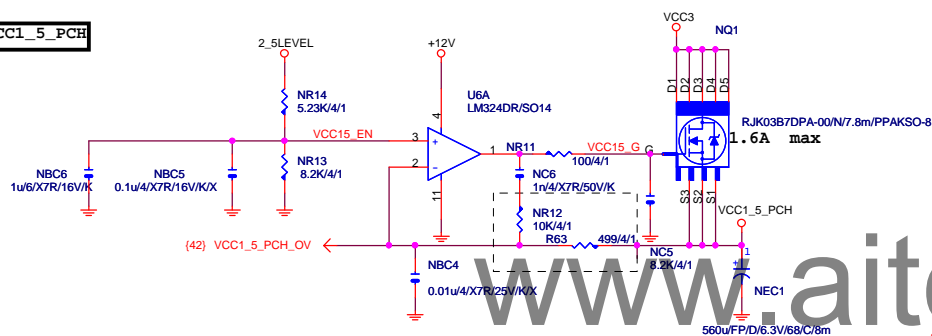
VCC1_05_PCH



ErP



VCC1_5_PCH

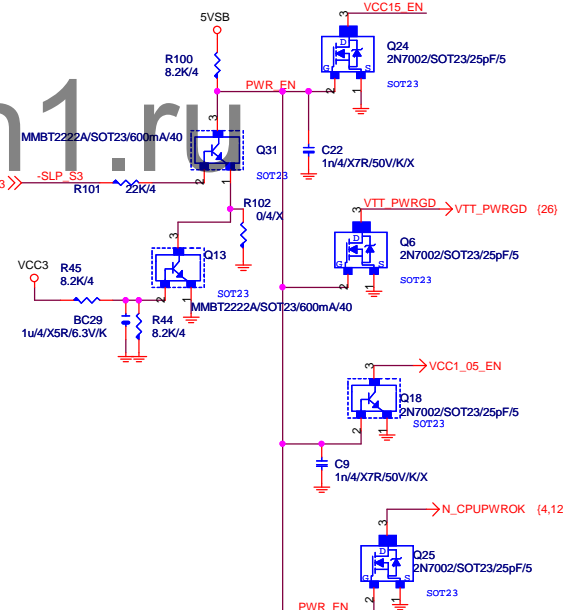
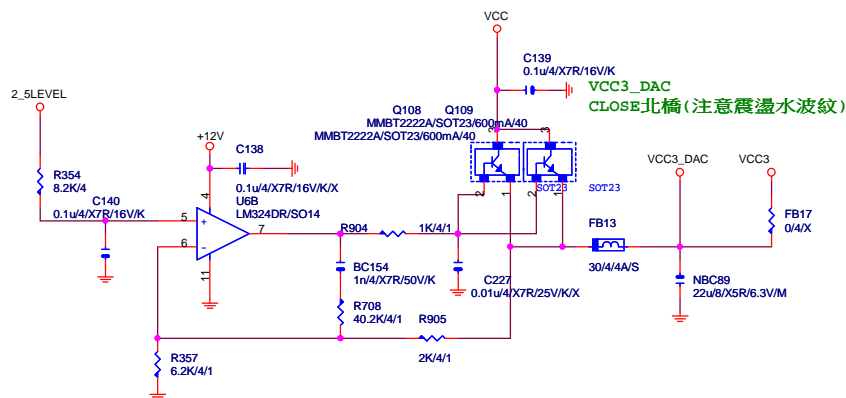


Rise/Fall max 50us
Rise:20% - 80%
Fall :2V- 0.8V

At least 10ms delay after 3VDUAL ready
Pop when PCH & SIO both use 3VDUAL-PCH

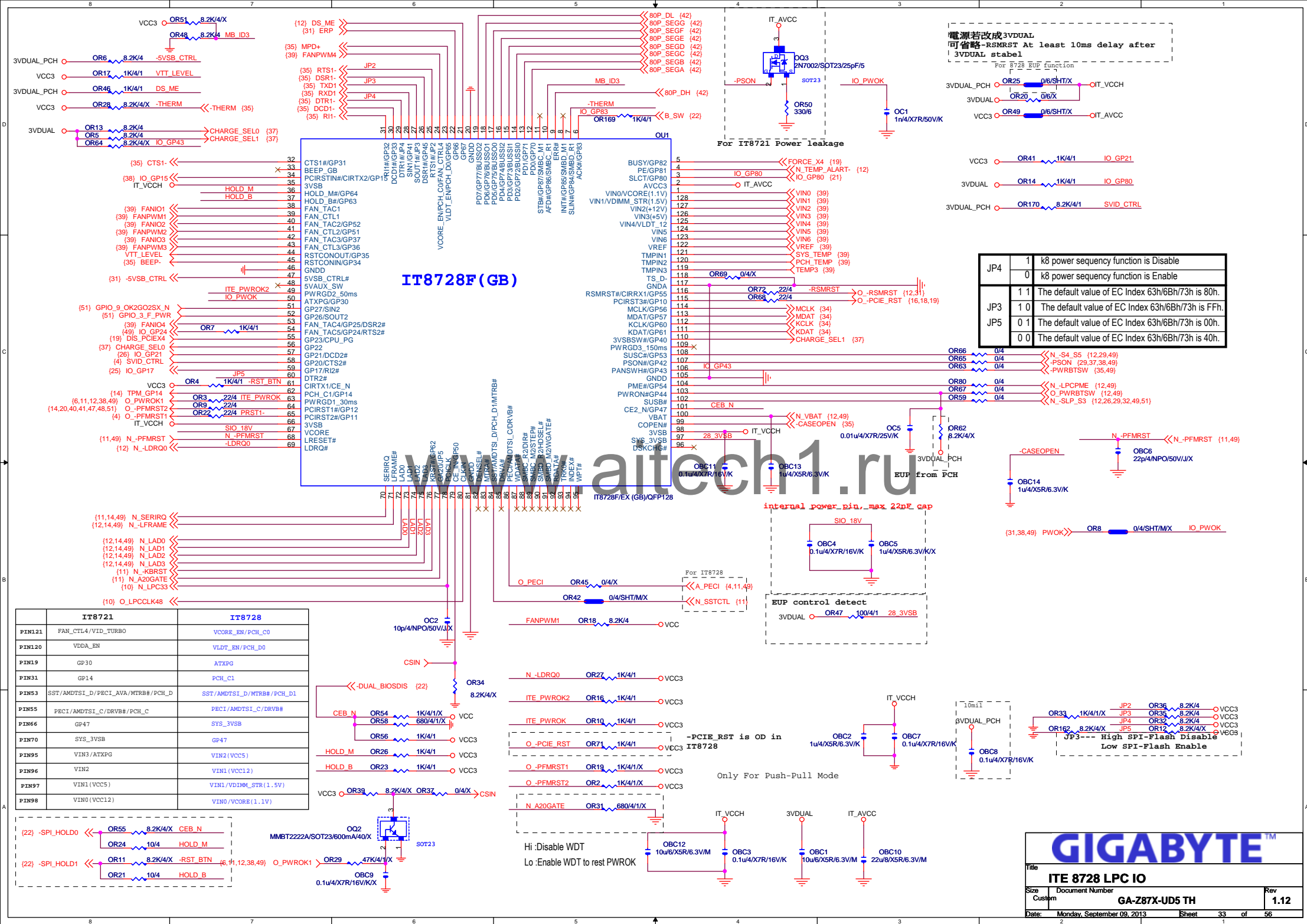
VCC3_DAC

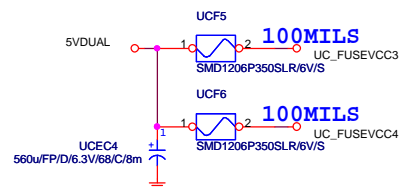
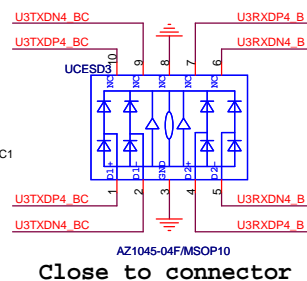
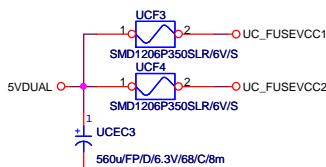
(3.3V/70mA+360uA)

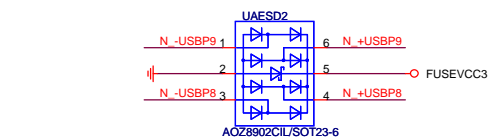
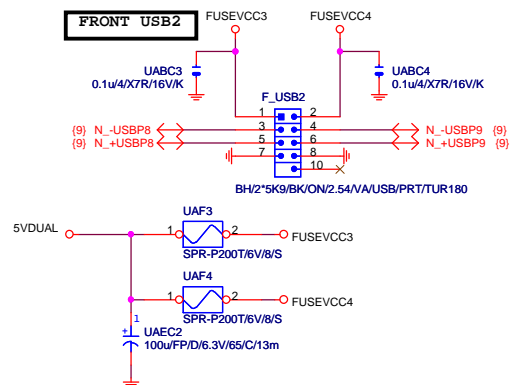


GIGABYTE™

Title			
VCC 1.05 PCH, VCC1.5 PCH, CC3 DAC			
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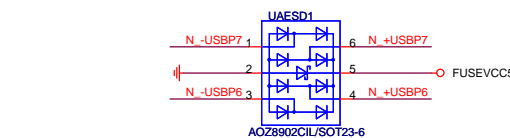
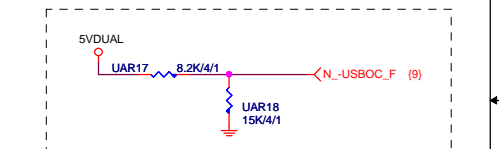




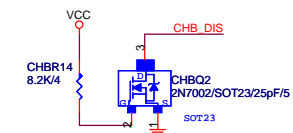
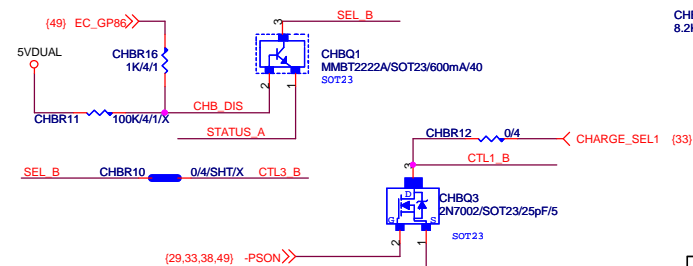
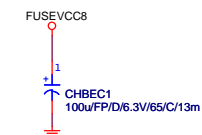
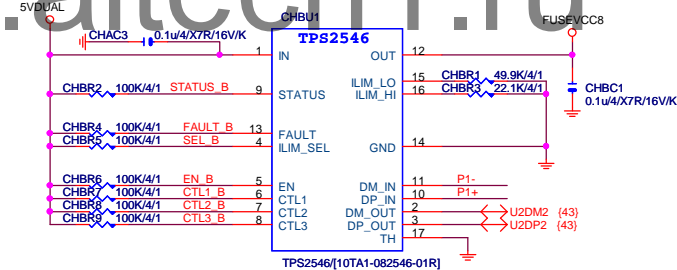
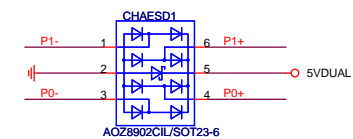
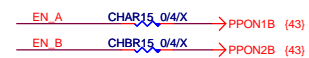
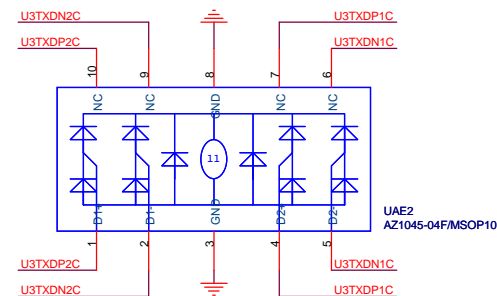
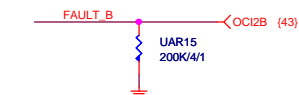


The schematic diagram illustrates the electrical connections for the USB3 module. Key components and connections include:

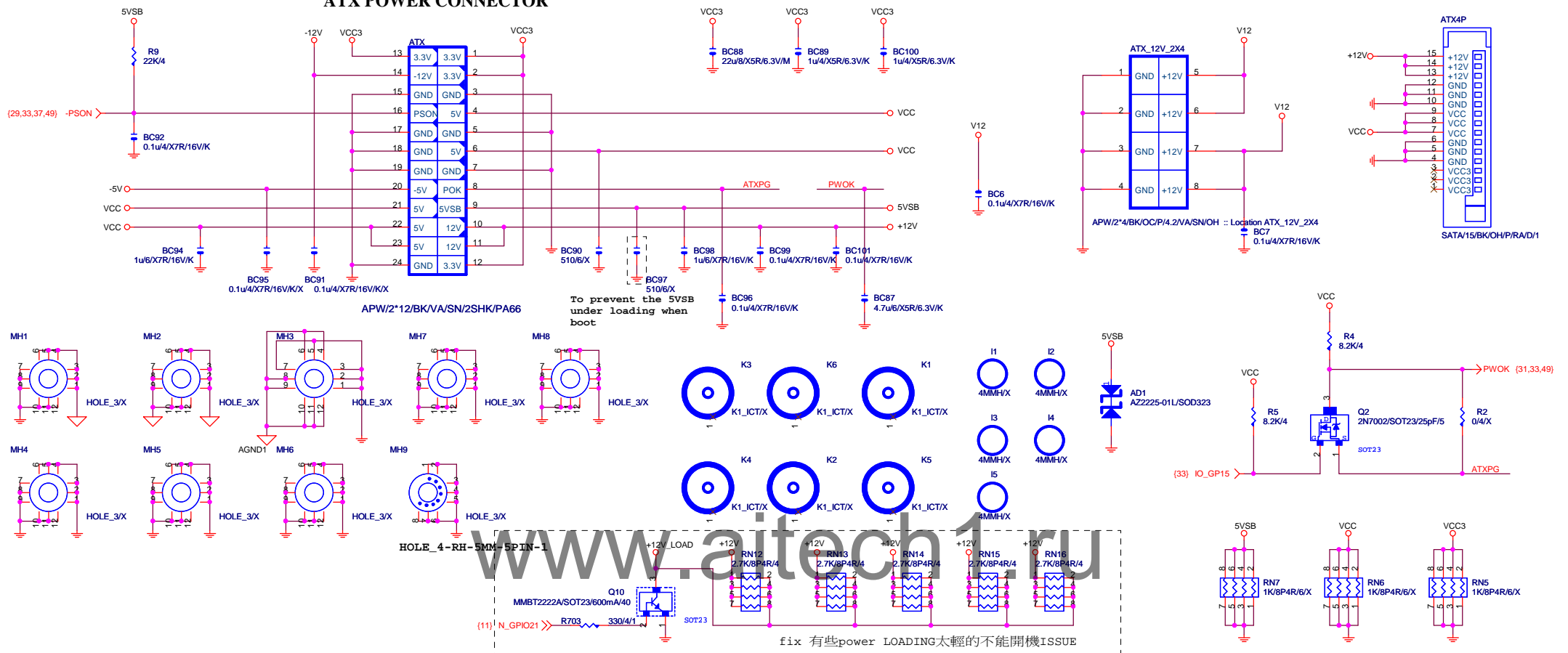
- UAB2C** and **UAB1**: Both are 0.1uF/4X7R/16V/K capacitors connected to ground.
- FUSEVCC5** and **FUSEVCC6**: Power supply connections for the module.
- UAF2** and **UAF1**: Both are SPR-P200T/6V/8/S capacitors connected to ground.
- UAC1**: A 100uF/FP/D/6.3V/65F/C/13m capacitor connected to ground.
- N_USBP6** and **N_+USBP6**: Data lines connected to the module pins.
- F_USB3**: A 10-pin connector with pins 1 through 10 labeled.
- BH/2*5K3/BK/ON/2.54/NA/USB/PTR/TUR180**: A label for the module or connector.



Title			
FRONT USB 2.0			
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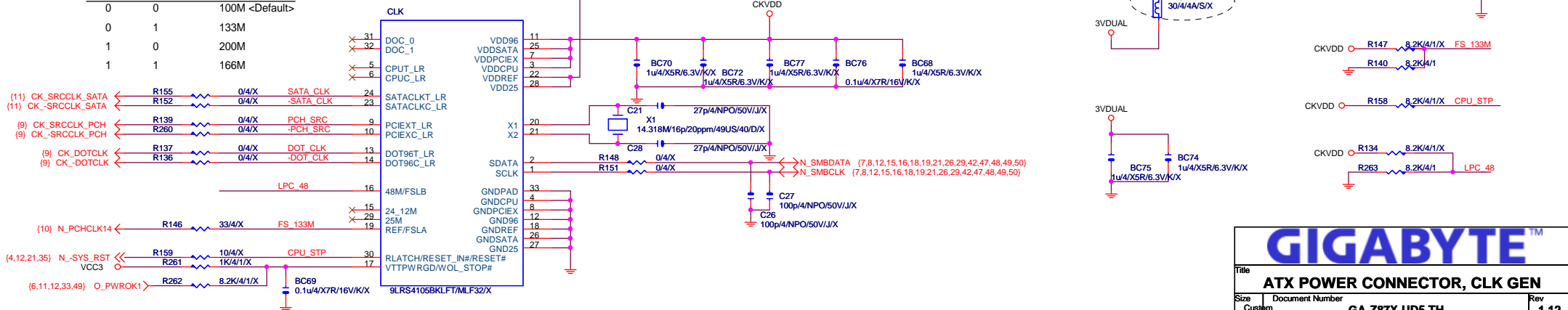
ATX POWER CONNECTOR



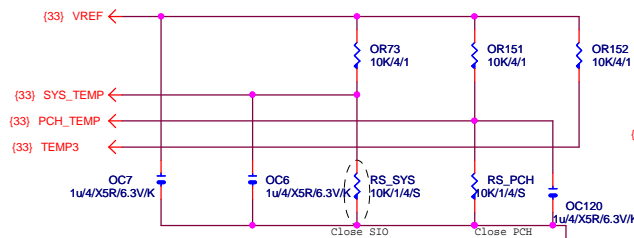
CLK GEN CK505

CPU Frequency Selection

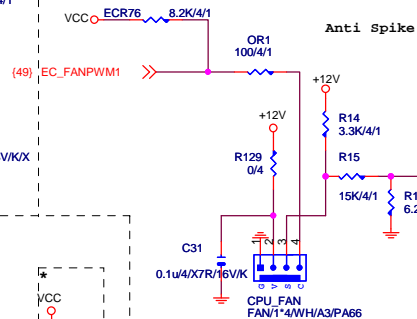
FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



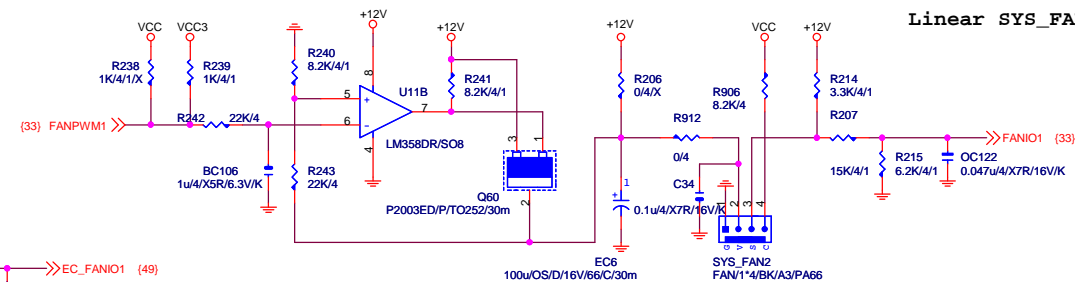
TEMP H/W MONITOR



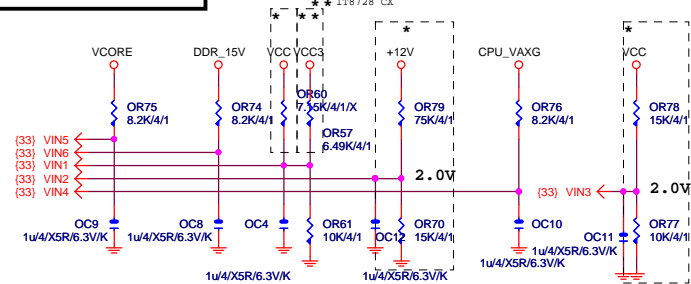
CPU SMART FAN



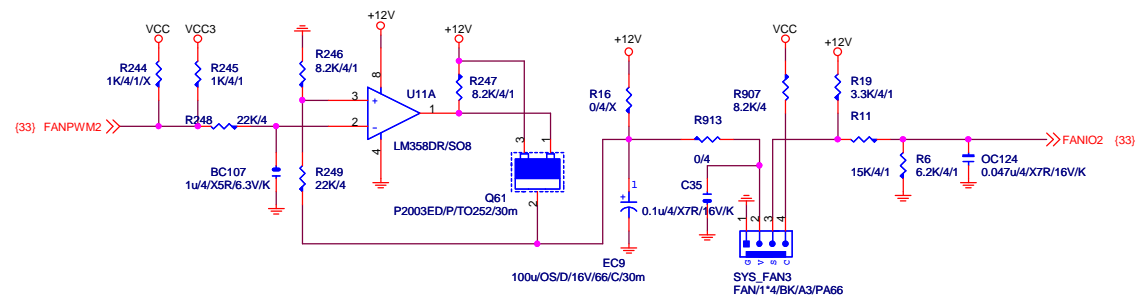
Linear SYS_FAN



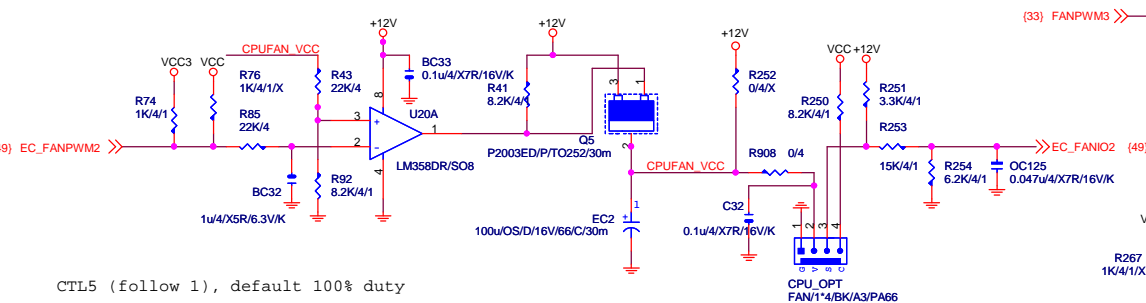
VOLTAGE-- H/W MONITOR



The division voltage of VIN2 & VIN3 must be around 2.9V

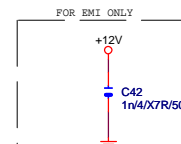
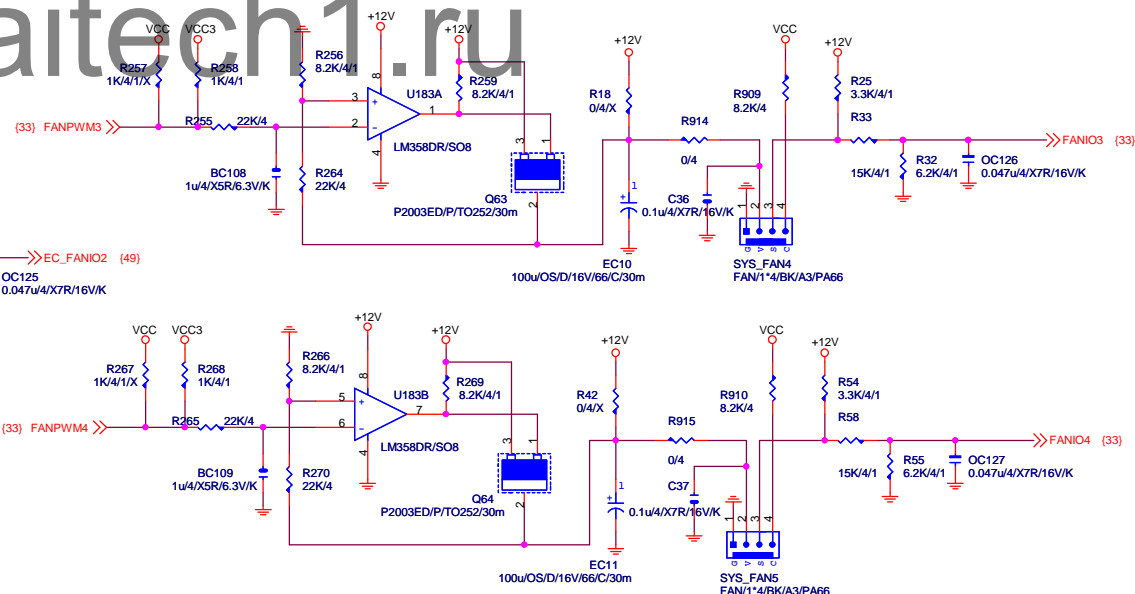
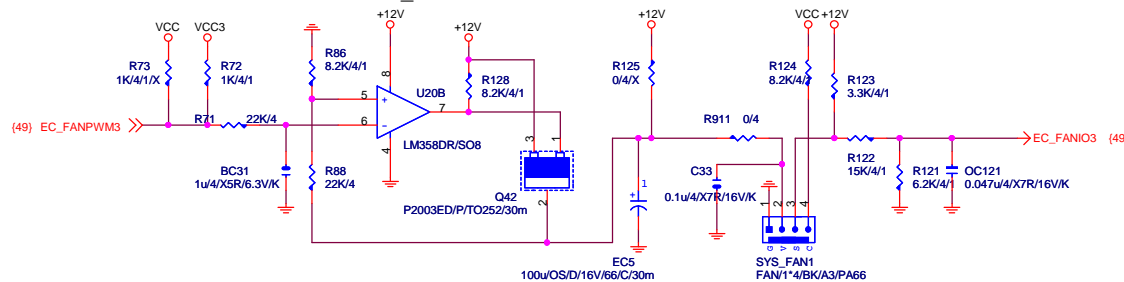


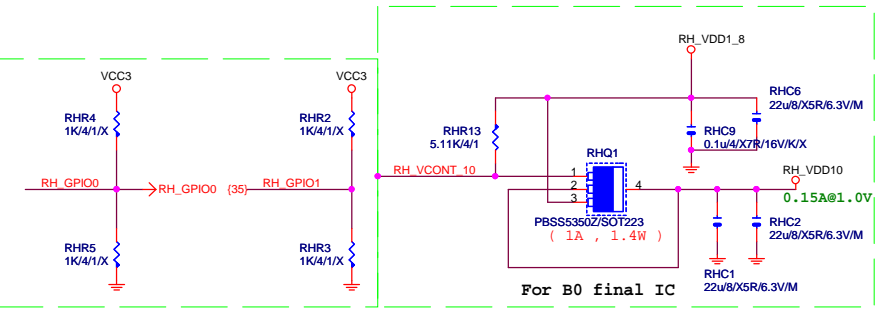
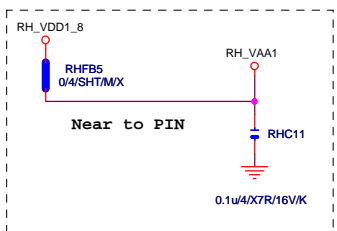
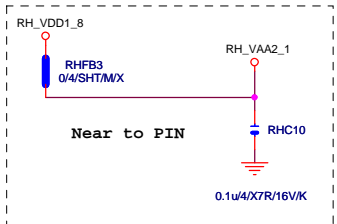
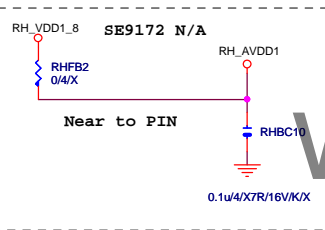
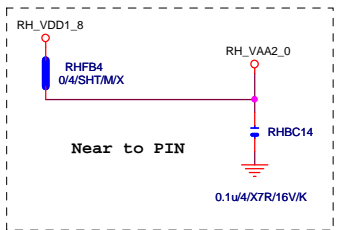
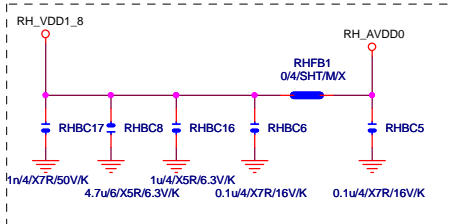
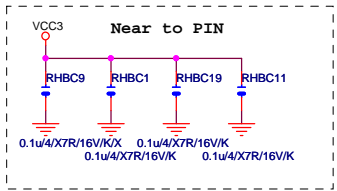
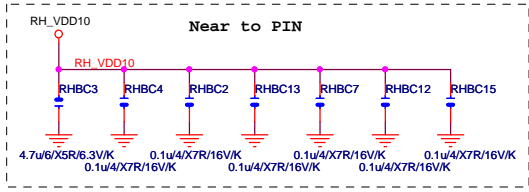
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CTL5 (follow 1), default 100% duty

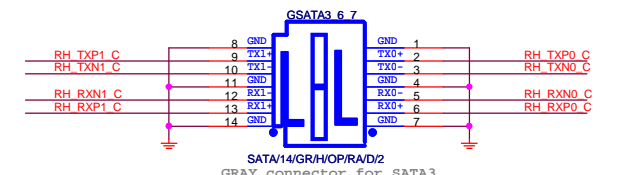
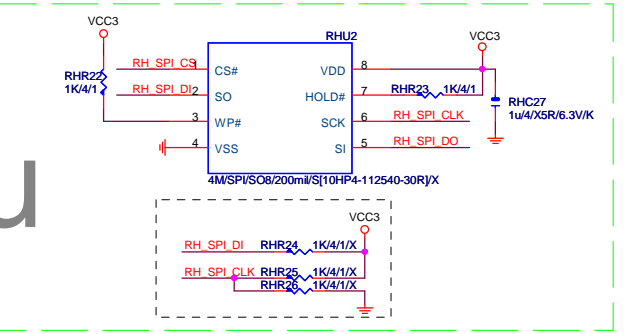
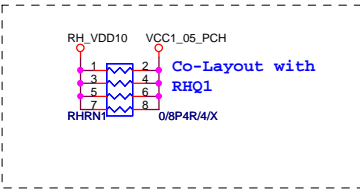
Linear SYS_FAN





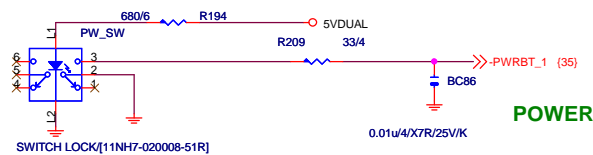
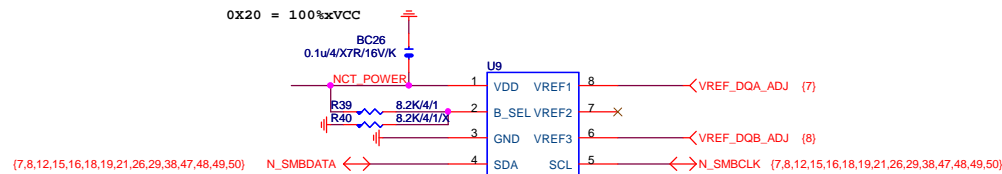
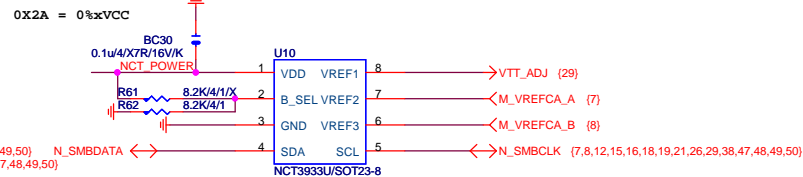
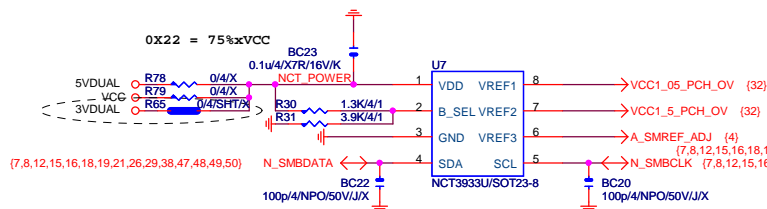
www.aitech1.ru

RH_TXP0	0.01u/4X7R/25V/K	RHC37	RH_TXP0_C
RH_TXN0	0.01u/4X7R/25V/K	RHC38	RH_TXN0_C
RH_RXN0	0.01u/4X7R/25V/K	RHC36	RH_RXN0_C
RH_RXP0	0.01u/4X7R/25V/K	RHC35	RH_RXP0_C
RH_TXP1	0.01u/4X7R/25V/K	RHC42	RH_TXP1_C
RH_TXN1	0.01u/4X7R/25V/K	RHC41	RH_TXN1_C
RH_RXN1	0.01u/4X7R/25V/K	RHC43	RH_RXN1_C
RH_RXP1	0.01u/4X7R/25V/K	RHC40	RH_RXP1_C



Marvell 9172 Power Requirements
 Analog 1.8V 230mA
 Core 1.0V 900mA
 I/O 3.3V 50mA

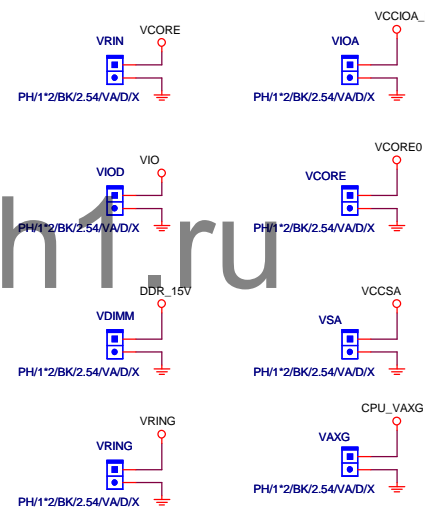
GIGABYTE™			
Title Marvell 9172 SATA 3.0			
Size	Document Number	Rev	
Custom	GA-Z87X-UD5 TH	1.12	
Date:	Monday, September 09, 2013	Sheet	41 of 56



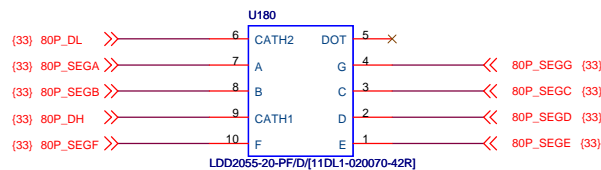
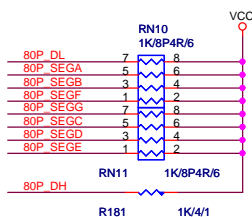
POWER

Reset

Clear CMOS

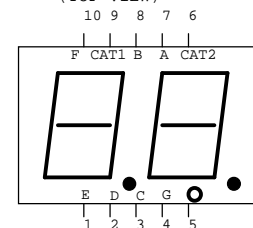


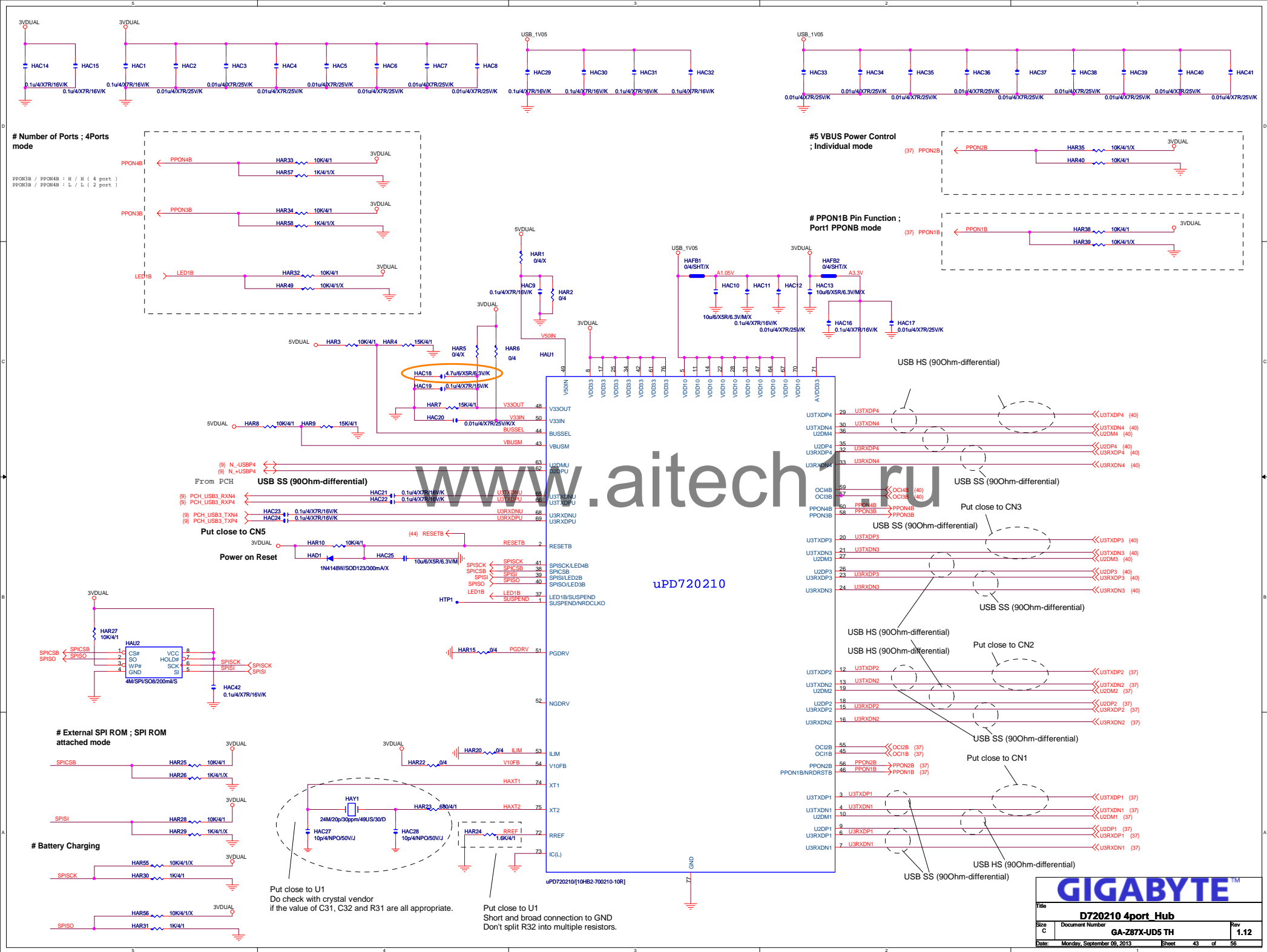
80 PORT



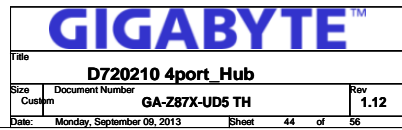
COMMON CATHODE

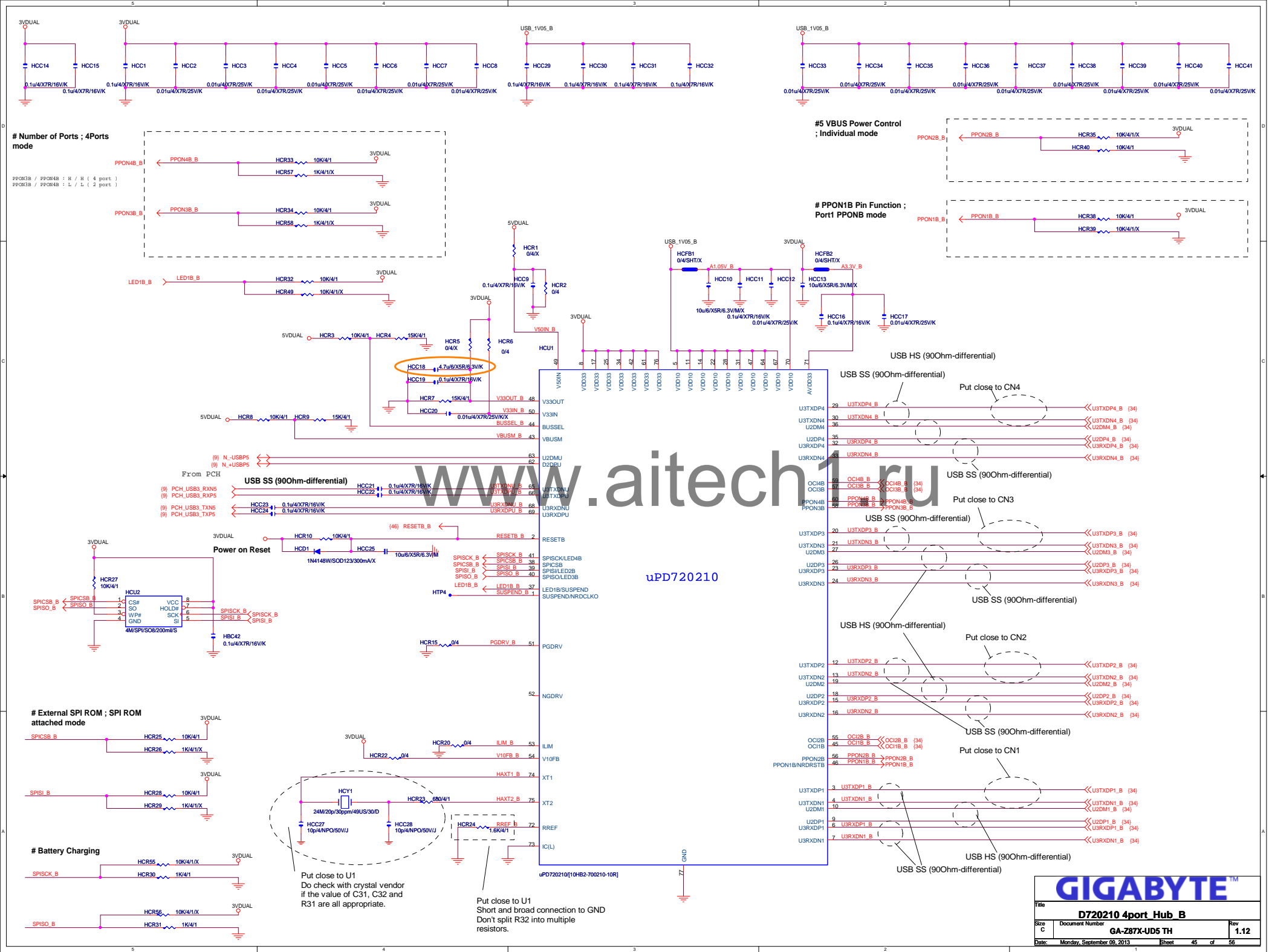
Physical Package
(TOP VIEW)



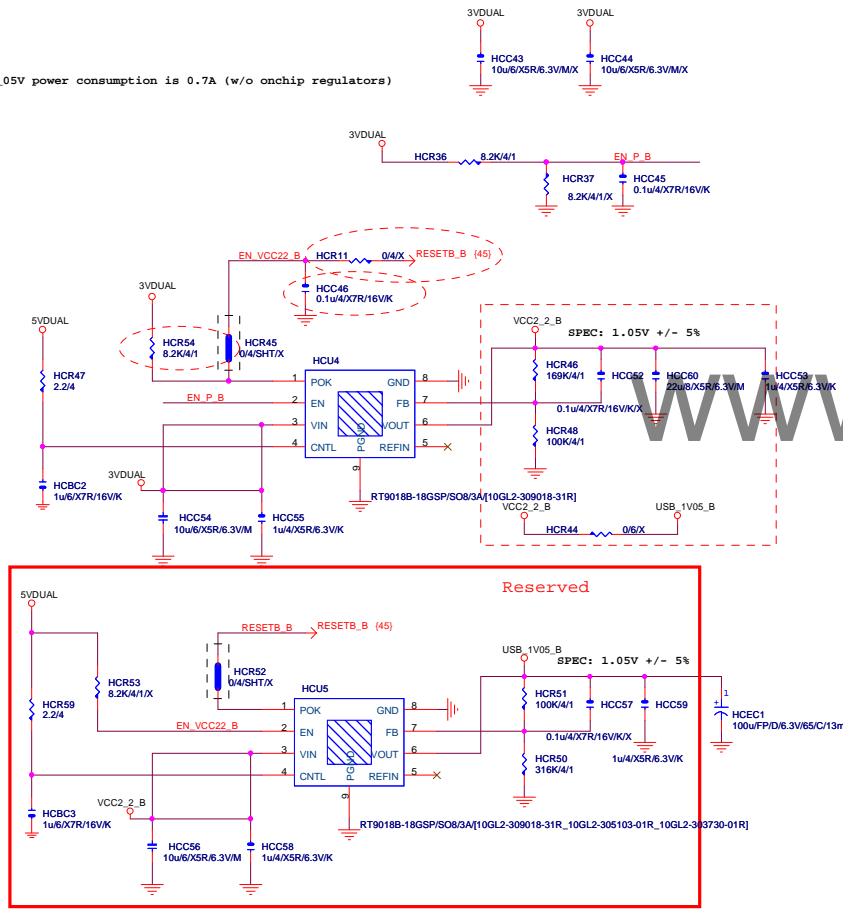


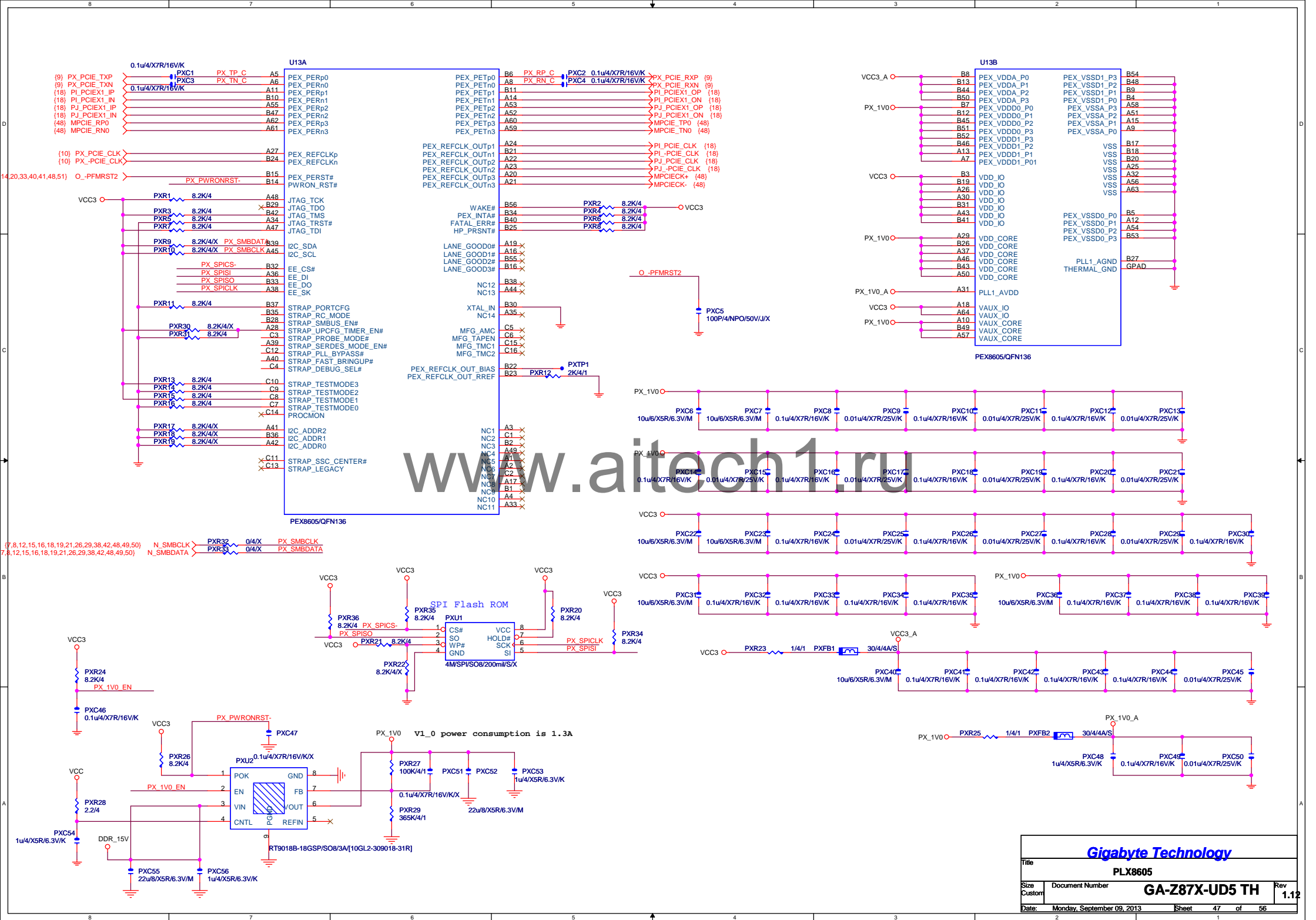
www.aitech1.ru

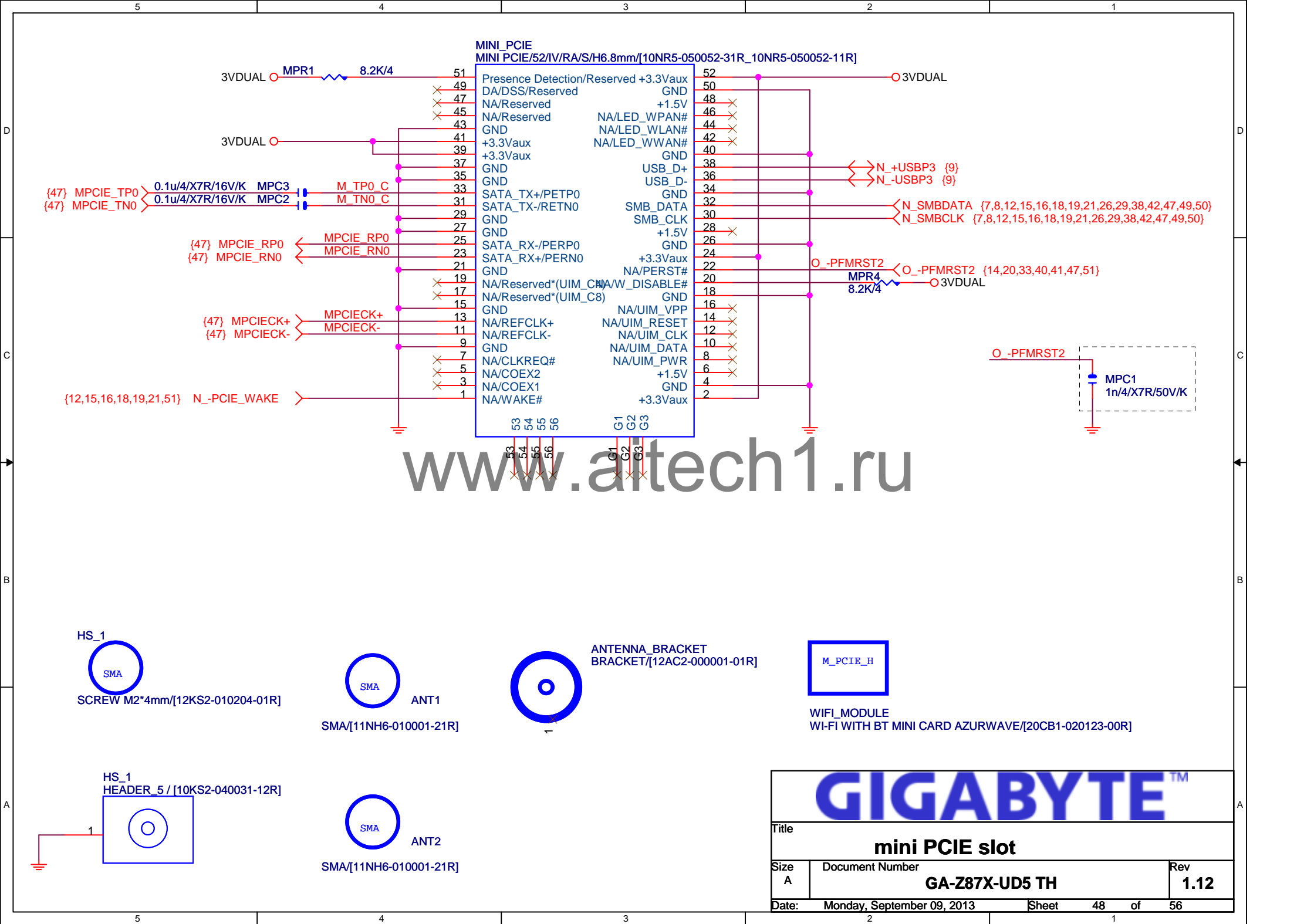


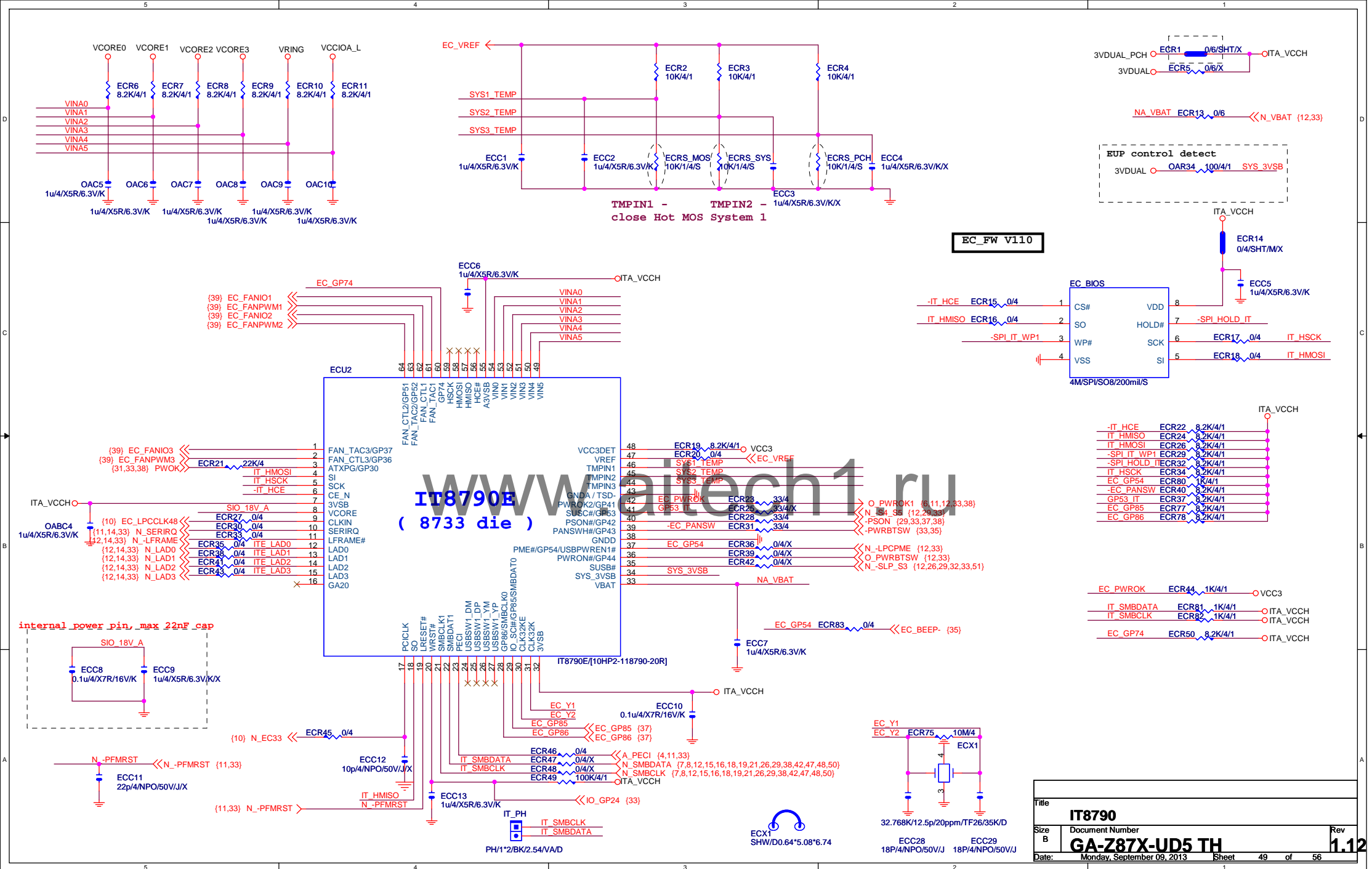


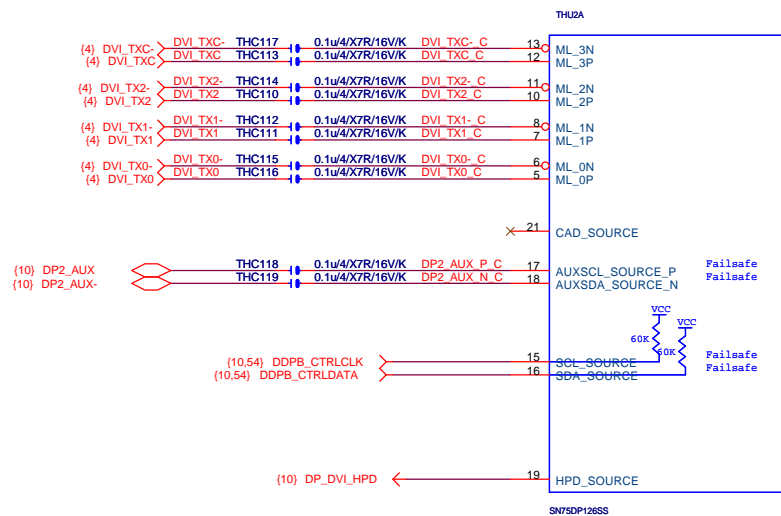
USB1_05V power consumption is 0.7A (w/o onchip regulators)



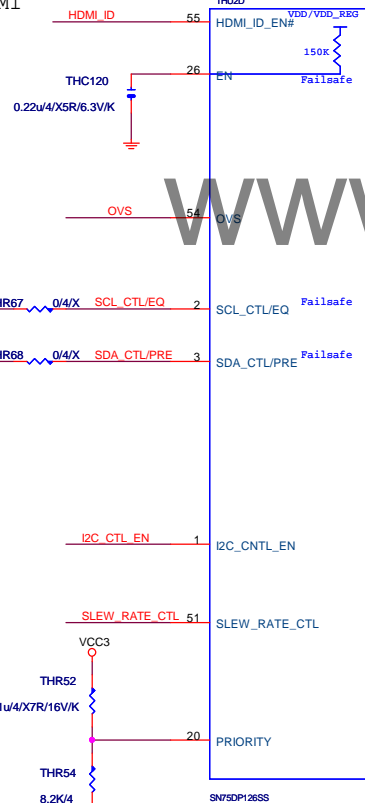




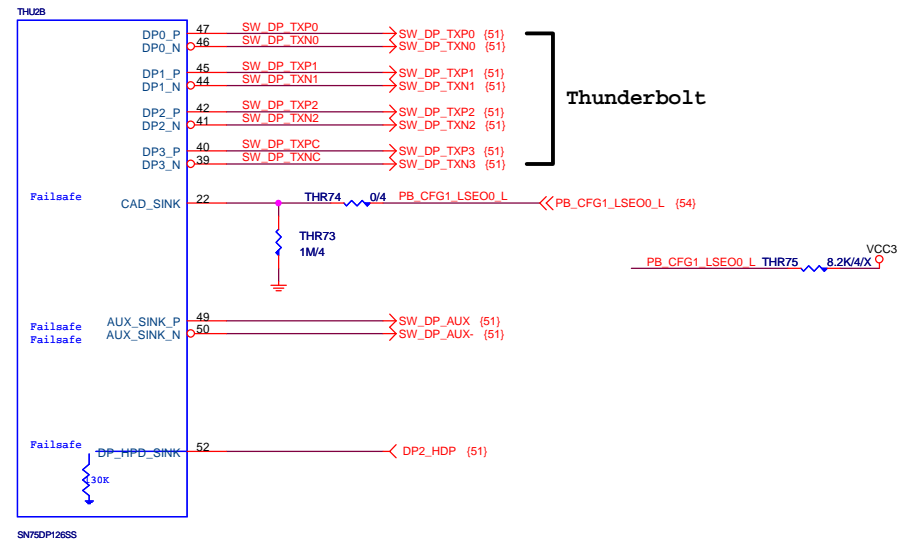




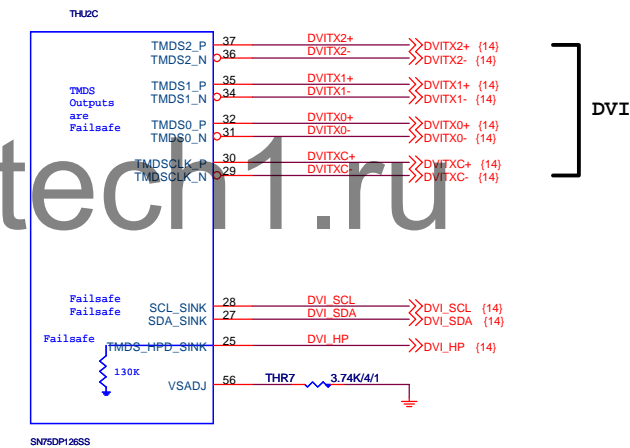
HDMI_ID
 LOW: HDMI
 HI: DVI



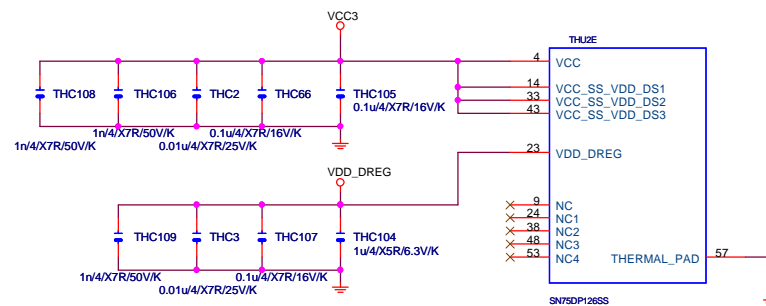
LOW: DP has Priority
 HI: DVI has Priority

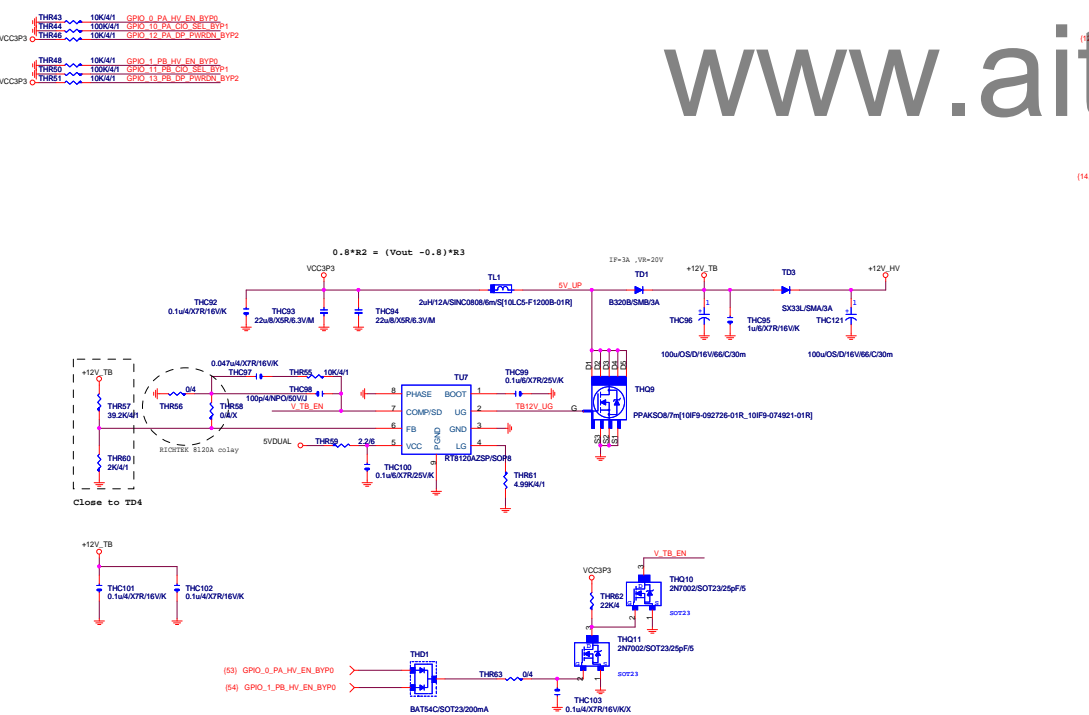
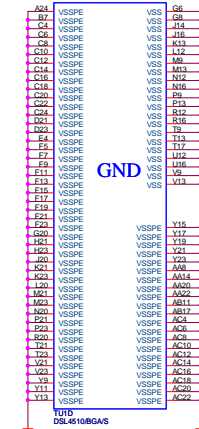
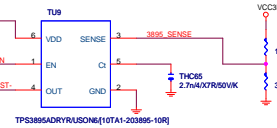
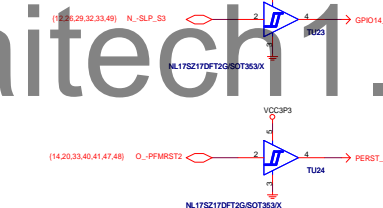
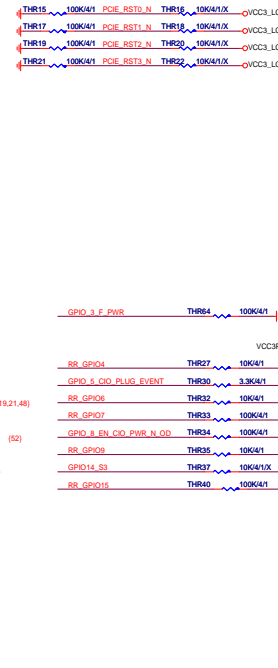
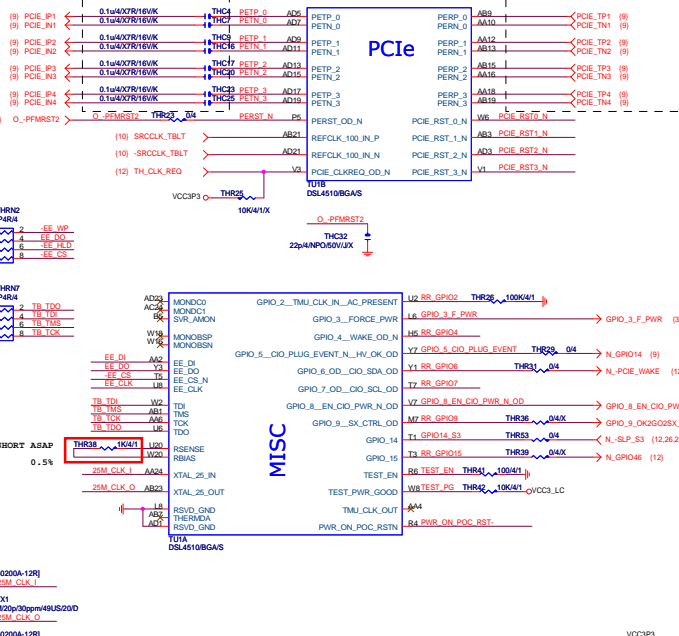
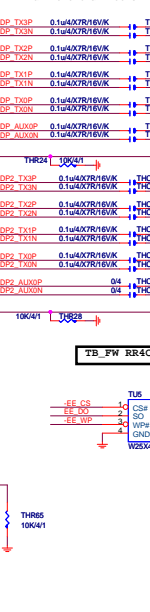


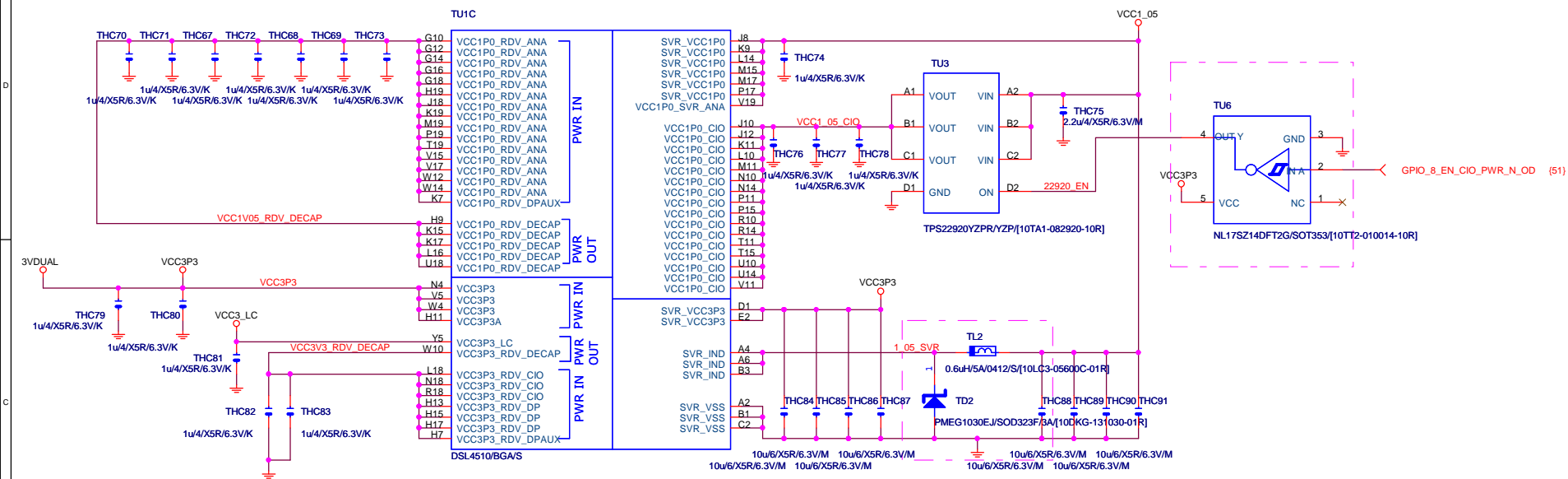
Thunderbolt



DVI

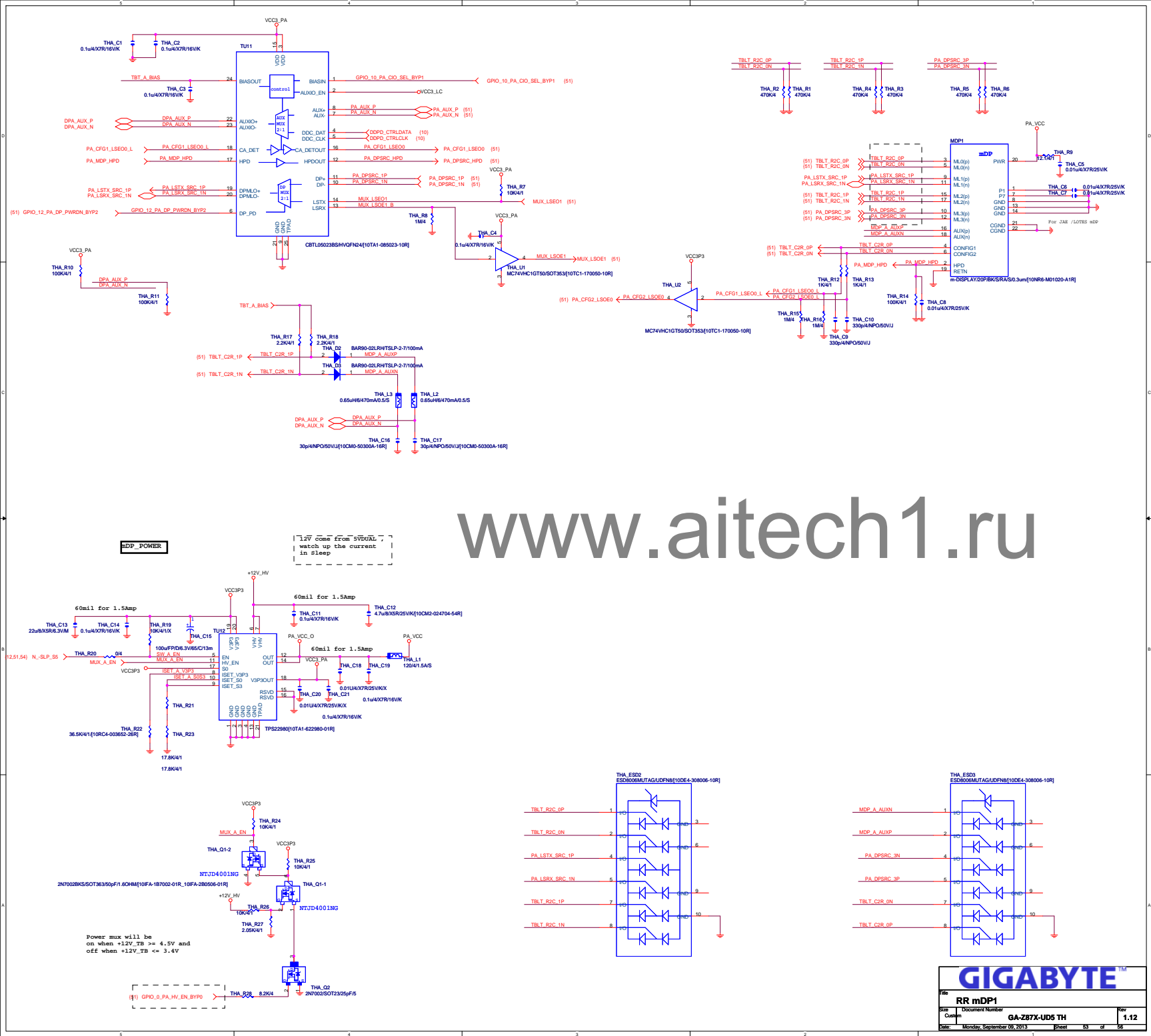


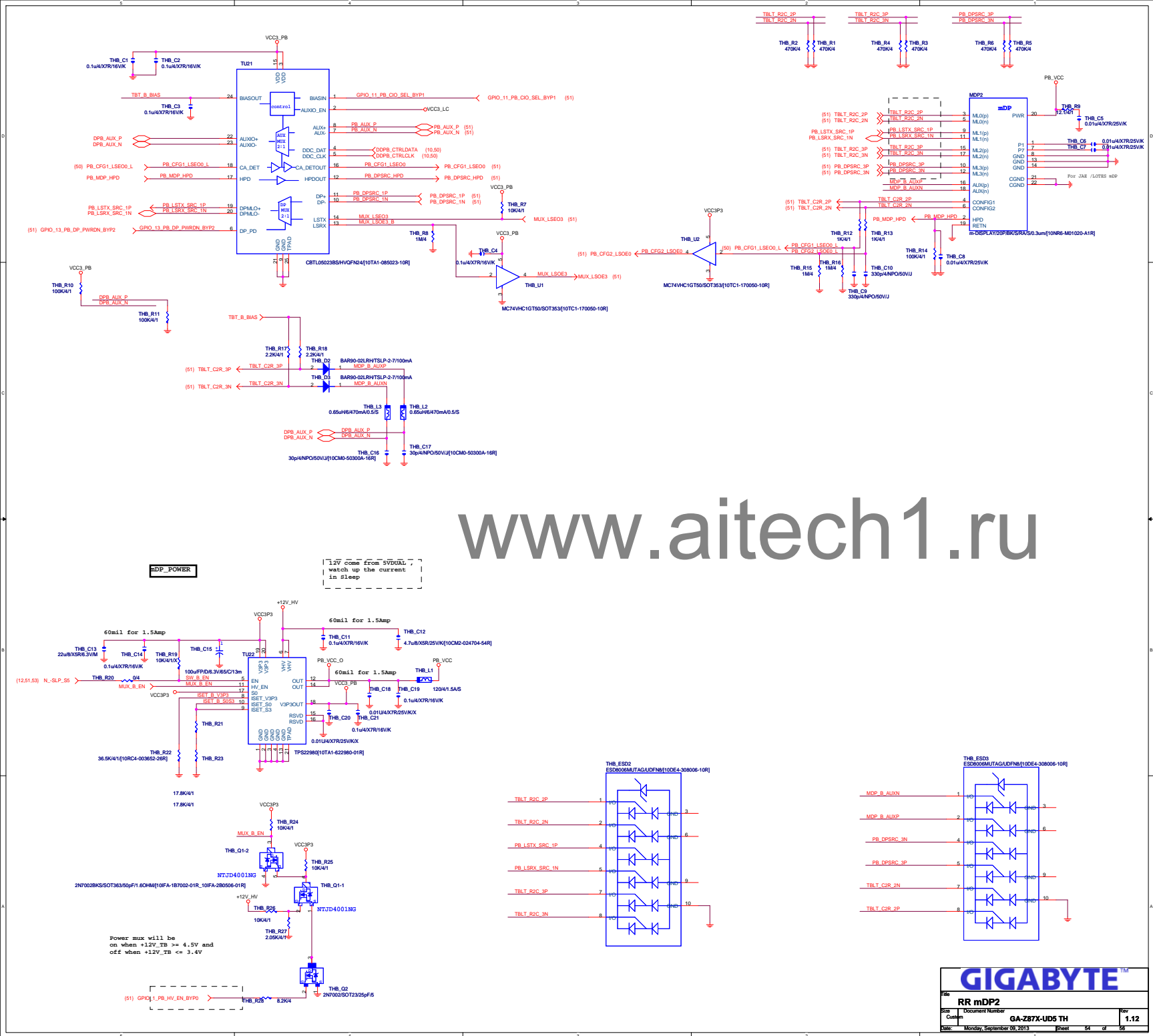
[illegible]



Power Consumption Table

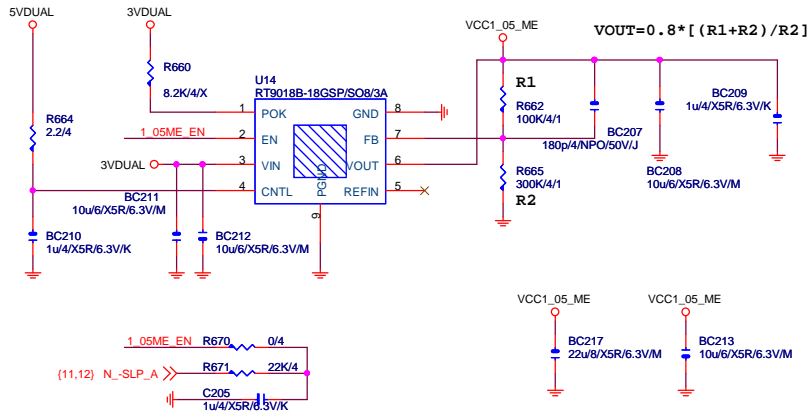
Sx Support Table



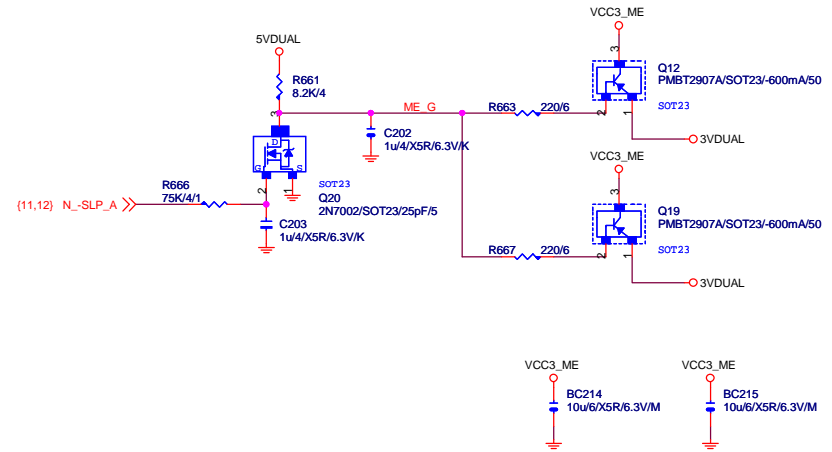


VCC1_05_ME

【技術通報R&D技術通報156】
(RICHTER), (NUVOTON), (EMC)做共用
PIN7分壓阻值須做修改為100K以上電阻值



VCC3_ME



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1

4

Super I/O ITE8720 GPIO Table

22

PWM各相位的擺法如下：



BIOS超電壓對應表：

2

散熱模組料號：
